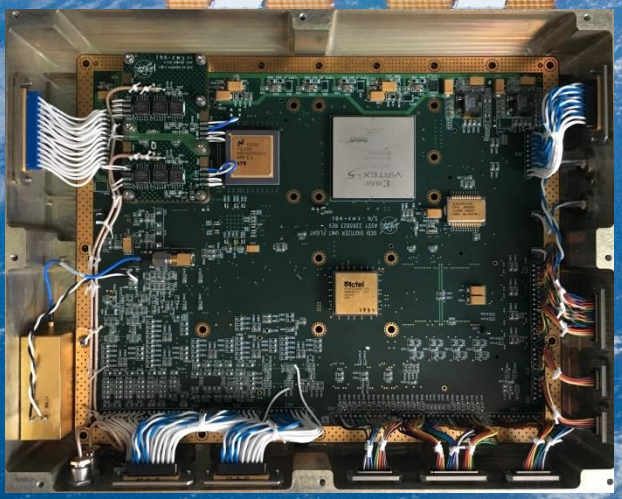
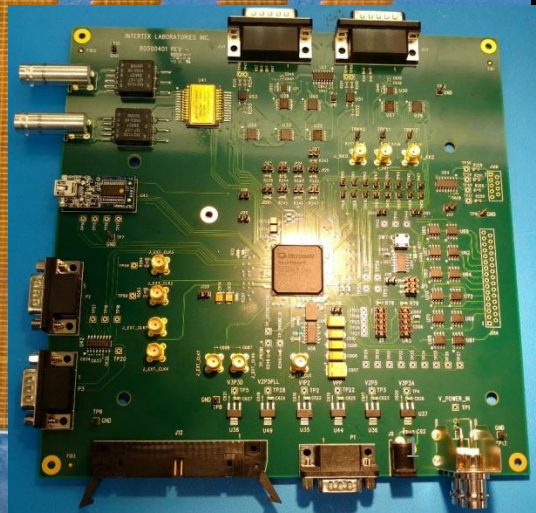
“Environmental Effects on Data Retention in Flash Cells”





60th Annual Fuze Conference, May 9-11, 2017, Cincinnati, Ohio.

""Environmental Effects on Data Retention in Flash Cells"

Rich Katz (NASA)
David Flowers (DMEA)
Keith Bergevin (DMEA)

Contact Information:
richard.b.katz@nasa.gov
david.flowers@dmea.osd.mil
keith.bergevin@dmea.osd.mil

Abstract

Flash technology is being utilized in fuzed munition applications and, based on the development of digital logic devices in the commercial world, usage of flash technology will increase. Antifuse technology, prevalent in non-volatile field programmable gate arrays (FPGAs), will eventually be phased out as new devices have not been developed for approximately a decade. The reliance on flash technology presents a long-term reliability issue for both DoD and NASA safety- and mission-critical applications. A thorough understanding of the data retention failure modes and statistics associated with Flash data retention is of vital concern to the fuze safety community.

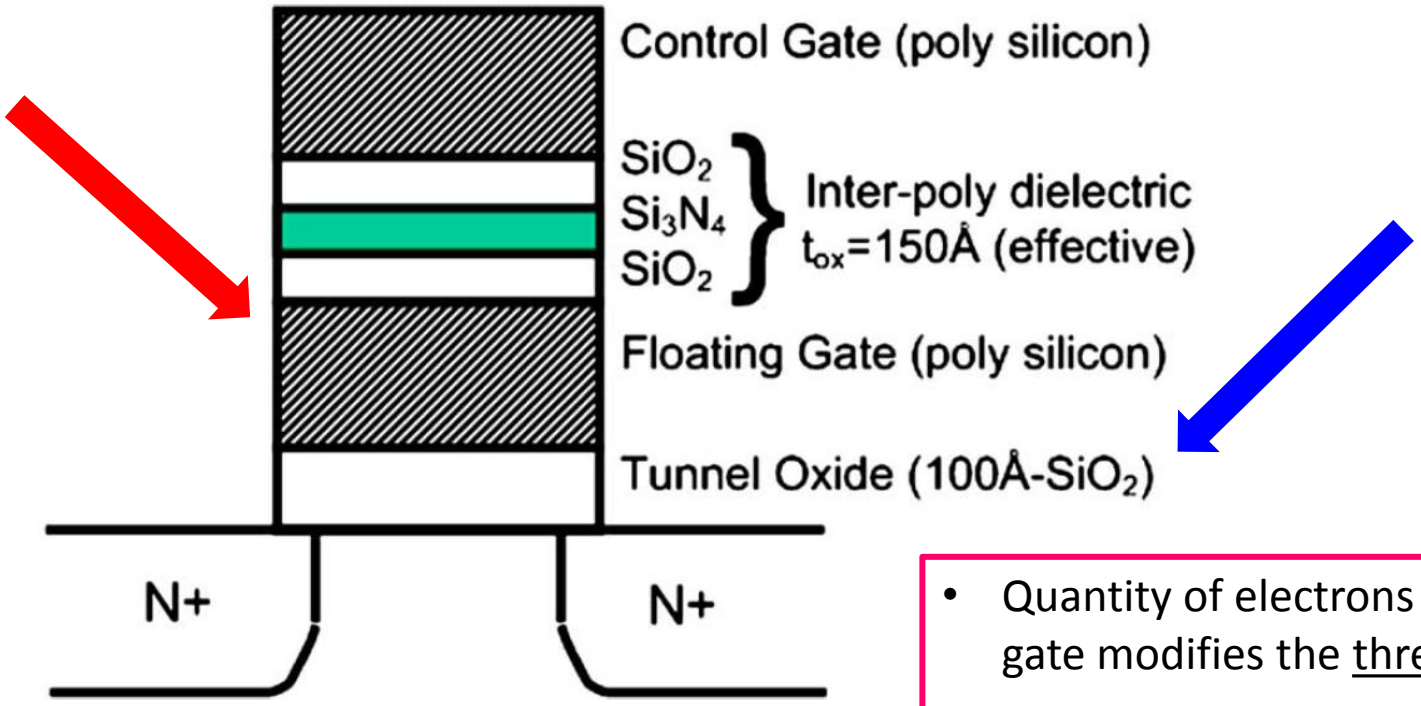
A key retention parameter for a flash cell is the threshold voltage (V_{TH}), which is an indirect indicator of the amount of charge stored on the cell's floating gate. This paper will present the results of our on-going tests: long-term storage at 150 °C for a small population of devices, neutron radiation exposure, electrostatic discharge (ESD) testing, and the trends of large populations (over 300 devices for each condition) exposed to three difference temperatures: 25 °C, 125 °C, and 150 °C.

Introduction and Agenda

- **Collaborative Effort Between NASA and DoD/DMEA**
- **Test Methods and Protocols**
- **DUT: Microsemi (Actel) A3P250L FPGA**
  - Common Technology Between spaceflight electronics and DoD fuze control circuitry.
- **Long-Term "Engineering Run" at +25 °C and +150 °C**
- **Threshold Voltage Distribution: Large Population (~1,100 DUTS)**
  - Part-to-Part Variability, Outliers, Trending
- **Results: Environmental Tests**
  - Temperature (+25 °C, +125 °C, and +150 °C)
  - Neutron Irradiation Susceptibility
  - Electrostatic Discharge (ESD) Susceptibility
  - Endurance (Erase/Program/Verify Cycles)

- **Additional Material and Data in the On-line Version of This Talk**

Threshold Voltage (V_T)



- Quantity of electrons stored on floating gate modifies the threshold voltage (V_T).
- Threshold voltage is the "turn on" voltage for the transistor.

Figure courtesy of Microsemi Corp.

Stress Induced Leakage Current (SILC)

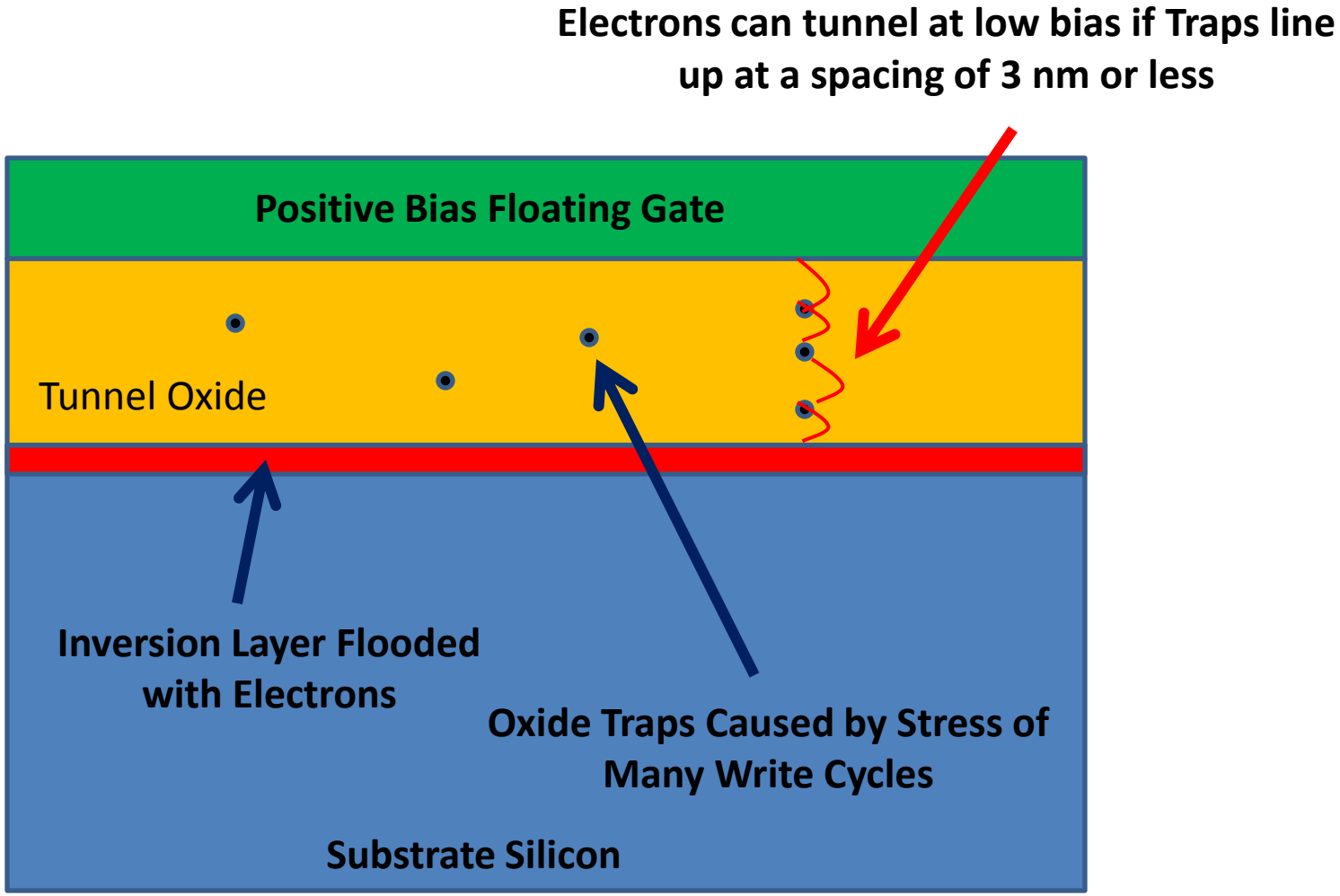


Chart courtesy of Microsemi Corp.

Smartfusion2 FPGA Flash Cell Data Retention Experiment

SmartFusion2 Retention Experiment Description

- Family: Microsemi SmartFusion2
- Model: M2S005FGG484
- Lot: SFCMJ17
- Date Code: 1420 0
- Quantity: 10 (9 exposed; 1 control)
- Pattern: smartfusion2_retention_0
- Stress: 1 Erase/Program/Verify Cycle
- Temp: 150 °C Bake
- Tests: "Verify" every 168 hours
- Start: March 3, 2017

Experiment Results

- All devices pass “Verify”
- No anomalies detected

Main Experiment Goals

- **The primary objective is to determine the probability of extrinsic flash cells in the population and to determine how that will limit the device's lifetime.**

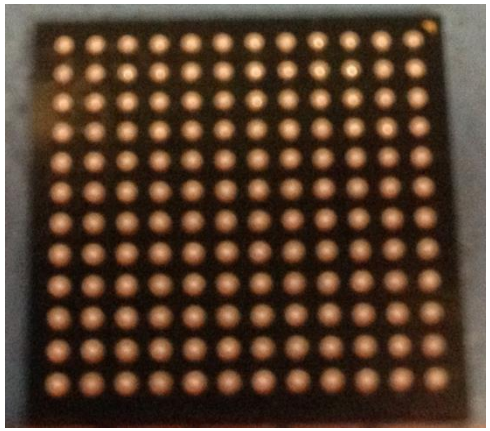
- **A secondary objective is to track the intrinsic populations lifetime which is a function of storage temperature.**

- **A third objective is to measure the flash cells' susceptibility to other environmental stresses.**
  - Neutron irradiation
  - Electrostatic Discharge (ESD)
  - Endurance (Erase/Program/Verify cycles)

Extrinsic cells are atypical; outliers in this context. Intrinsic cells are typical and have common characteristics through the population.

Description of DUTs (A3PL)

- **Microsemi (Actel) A3P250L FPGA**
  - Relatively small FPGA
  - PBGA (Plastic Ball Grid Array) Package (FG144)
  - Single Foundry for all DUTs
  - Most parts from one wafer lot (QLWY8)
    - Small number of DUTs from a second wafer lot (QLG10)



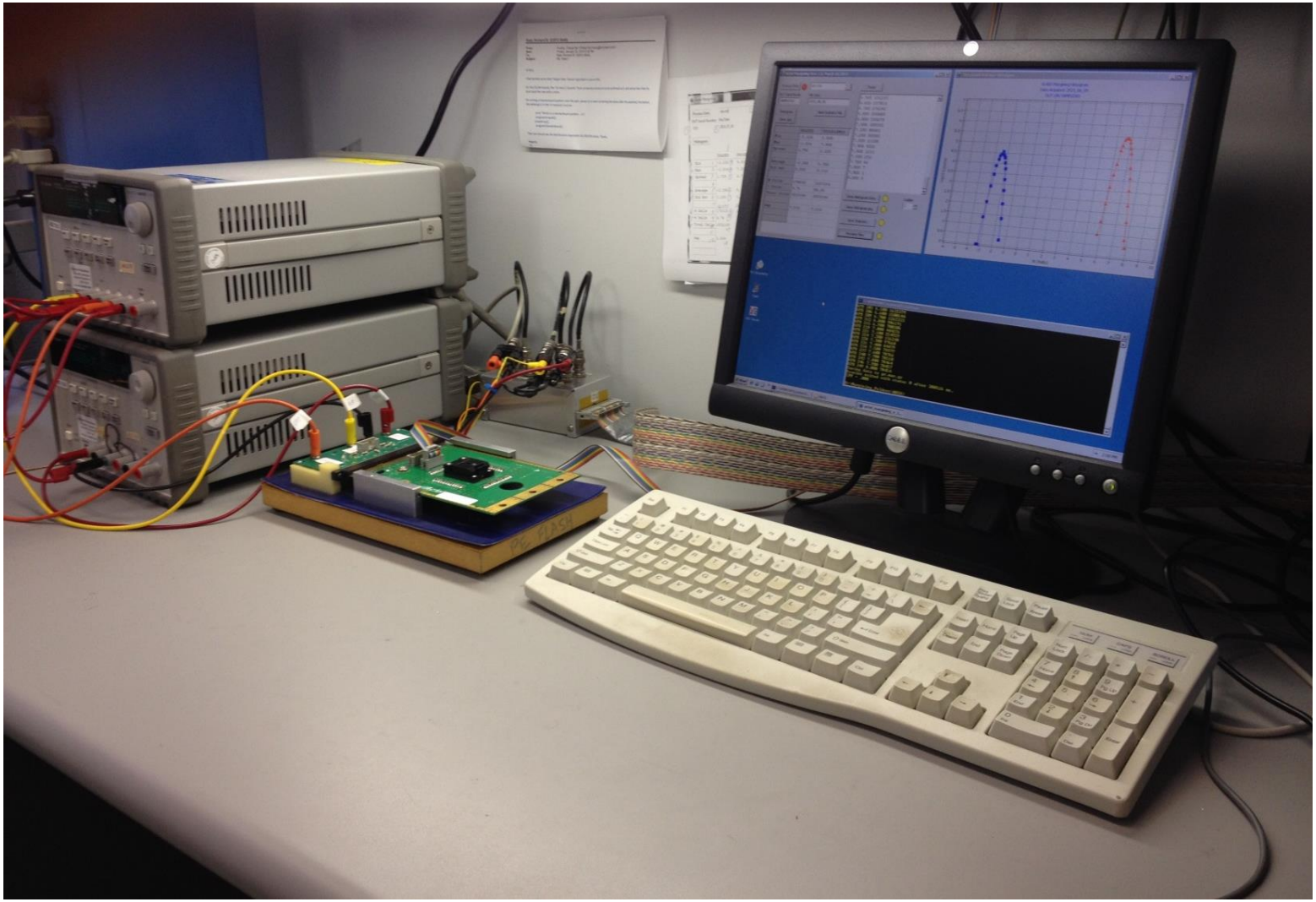
0.5”

- **9 Logic Designs Used**
  - No artificial test structures
  - Logic blocks designed by different authors and styles (including macro generators)

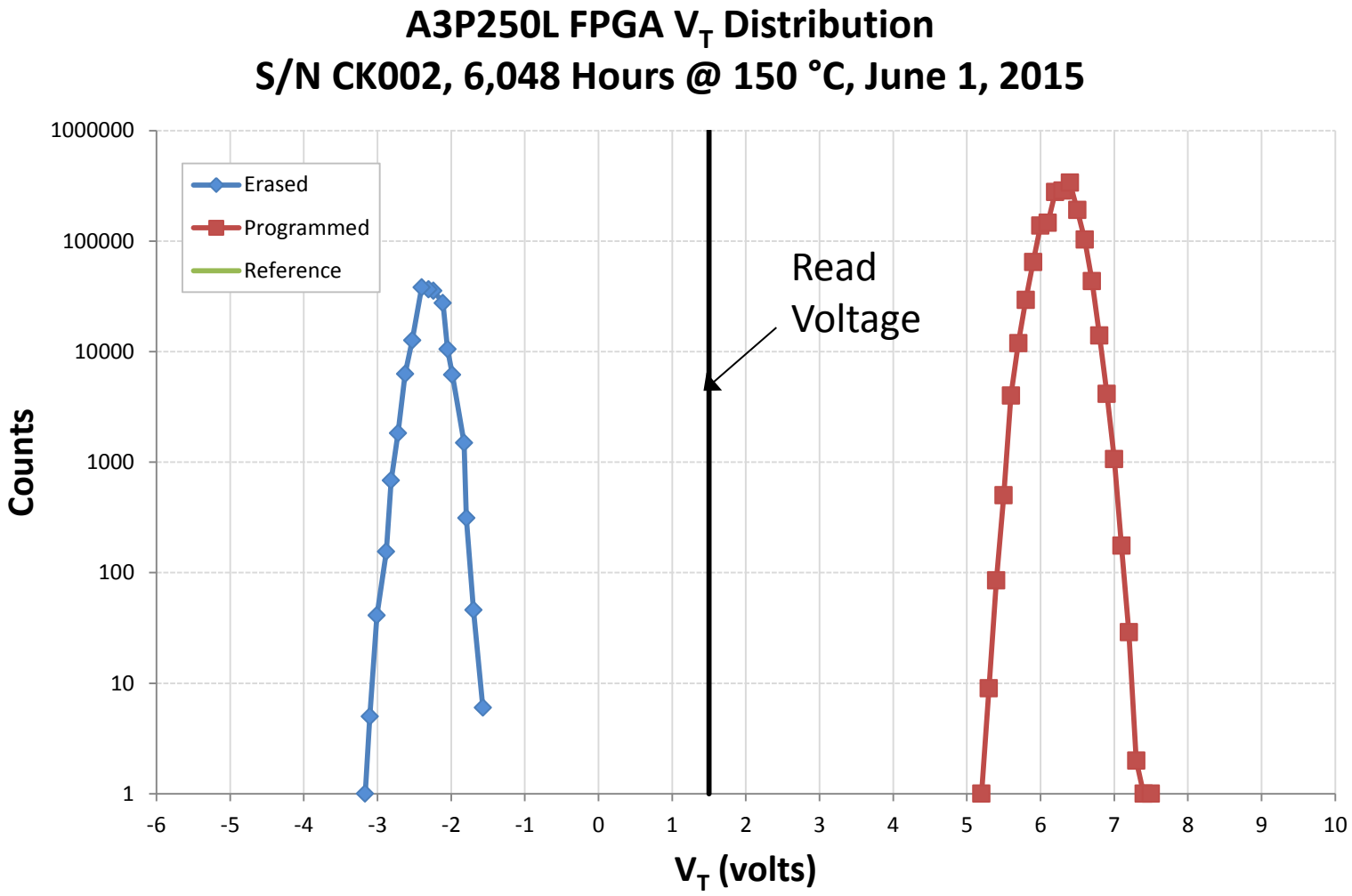
- **10 Erase-Program-Verify Cycles for Each Device**
  - Realistic stress for our applications.
  - Manufacturer’s rating: 500 cycles

- **Complements and Extends work by Sandia National Labs**
  - Sandia is a Department of Energy organization that has previously investigated flash cell reliability. See references at the end of this presentation.

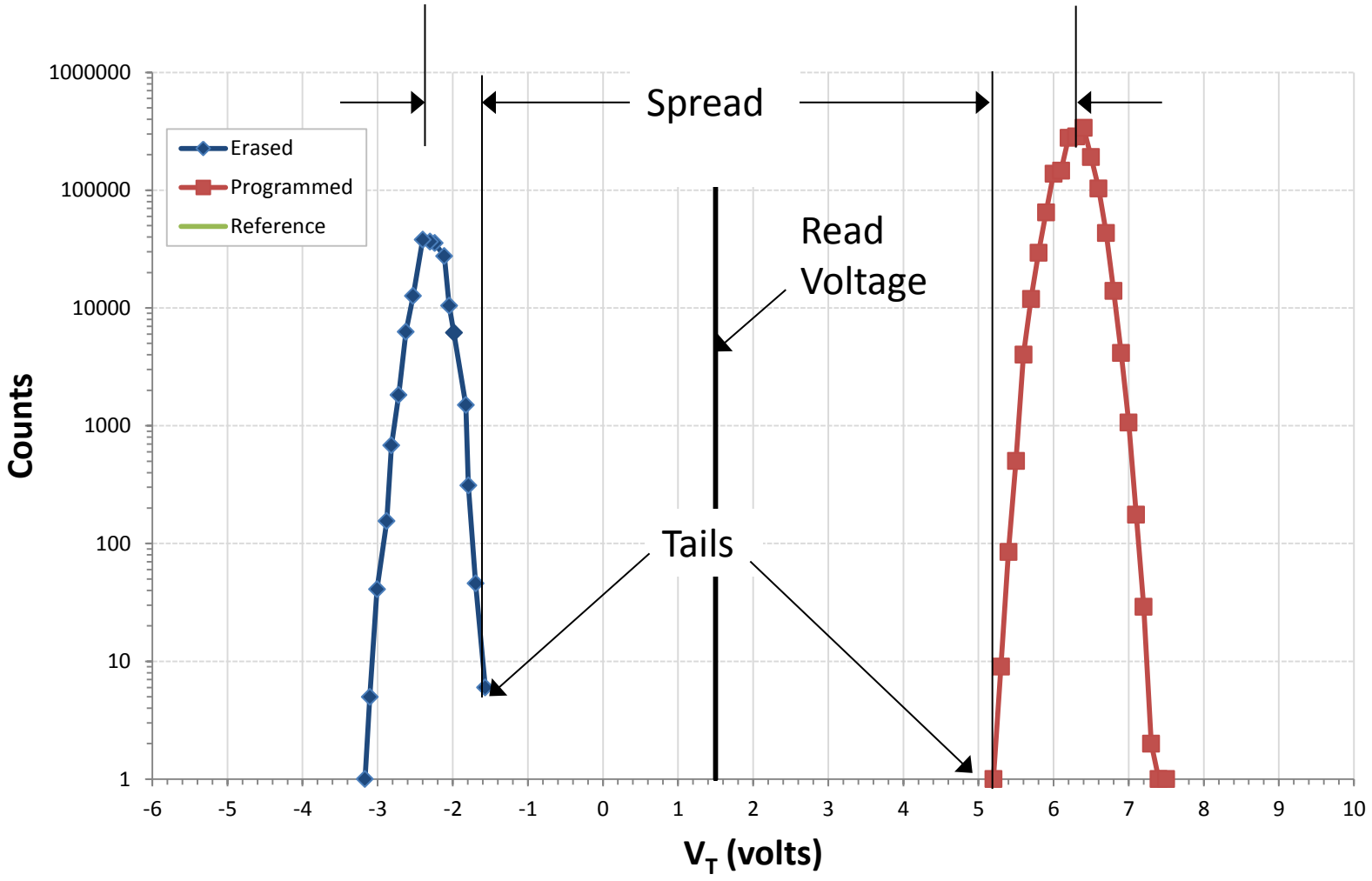
Test Station for A3P250L FPGA



Sample V_T Distribution in an FPGA



Population Analysis: Metrics



A3PL FPGA Flash Cell Data Long Term Trending Experiment

Long-Term "Engineering Run"

- **Goals**
  - Develop and refine test methods, procedures, and analysis tools and techniques
  - "Look ahead" at device response and behavior of intrinsic population

- **DUTS: 6 A3P250L FPGAs (3 each from two lots)**
  - 4 DUTs baked at 150 °C
    - One part failed at ~12,000 hours; second part failed at ~16,000. Neither failure appears to be flash cell related.
  - 2 DUTs kept at room temperature (control samples)
    - No failures.

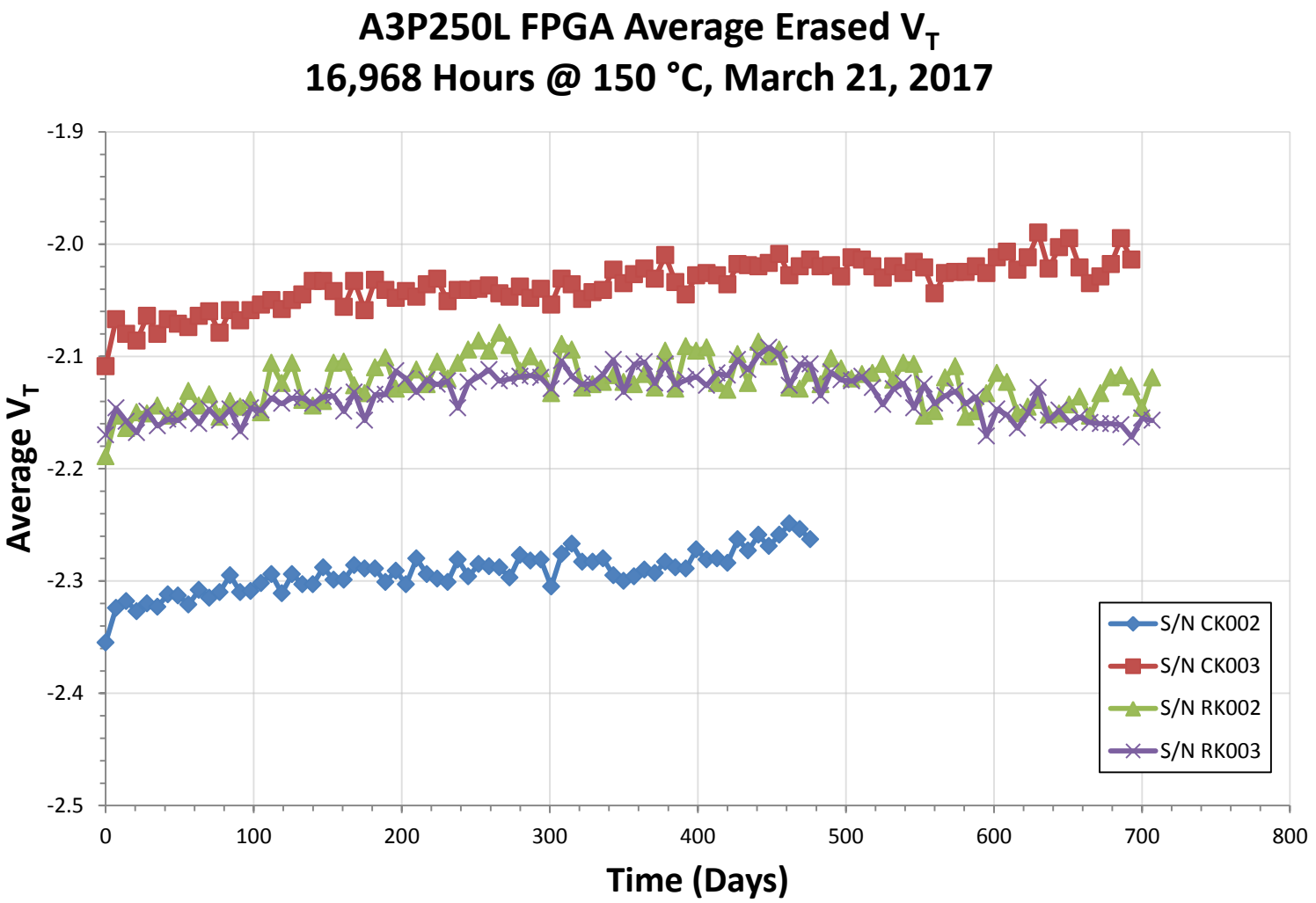
- **16,968 hours (~1.94 years) at 150 °C**

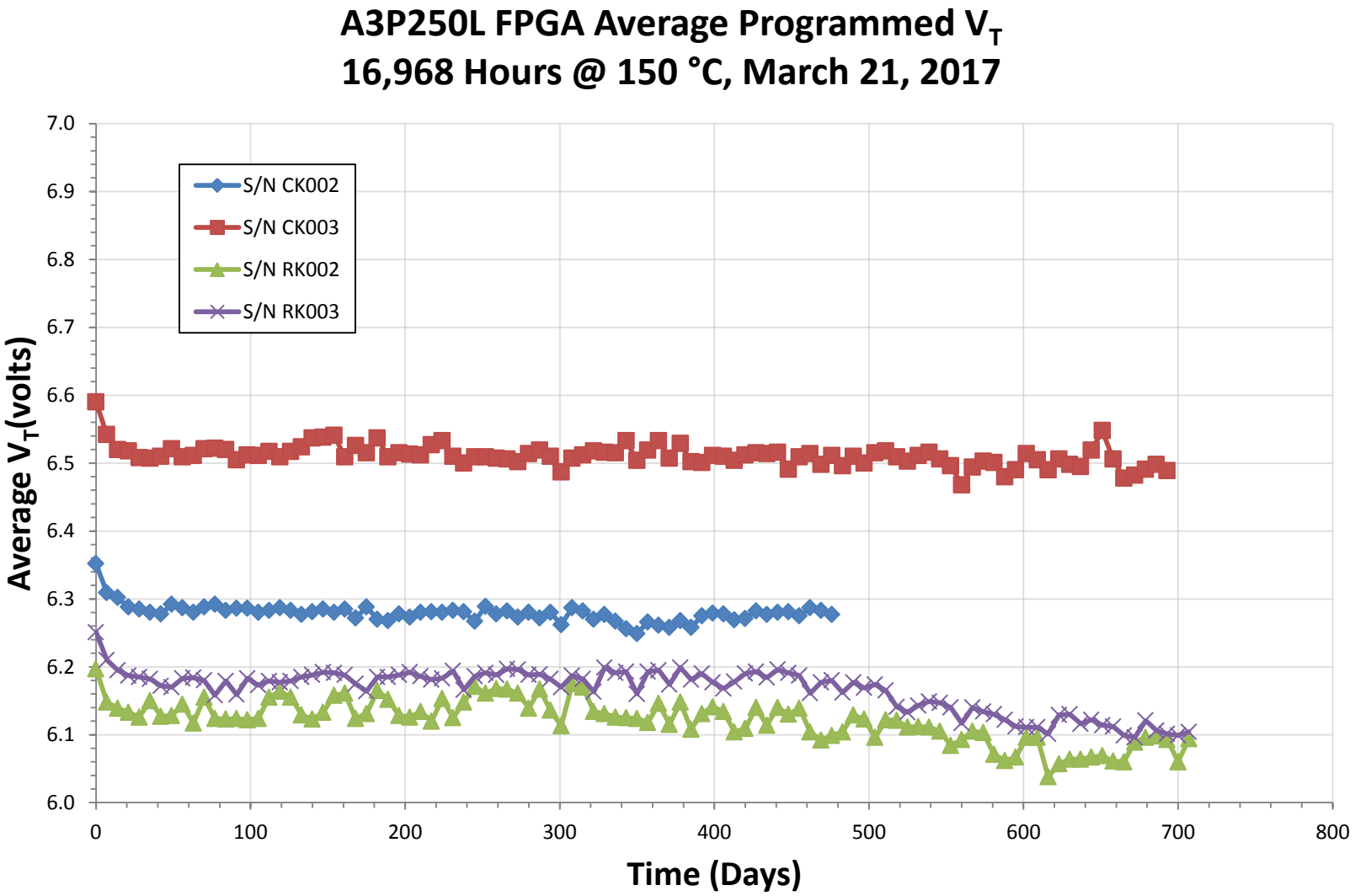
Erased Cell Data Retention at 150 °C Performance vs. Specification

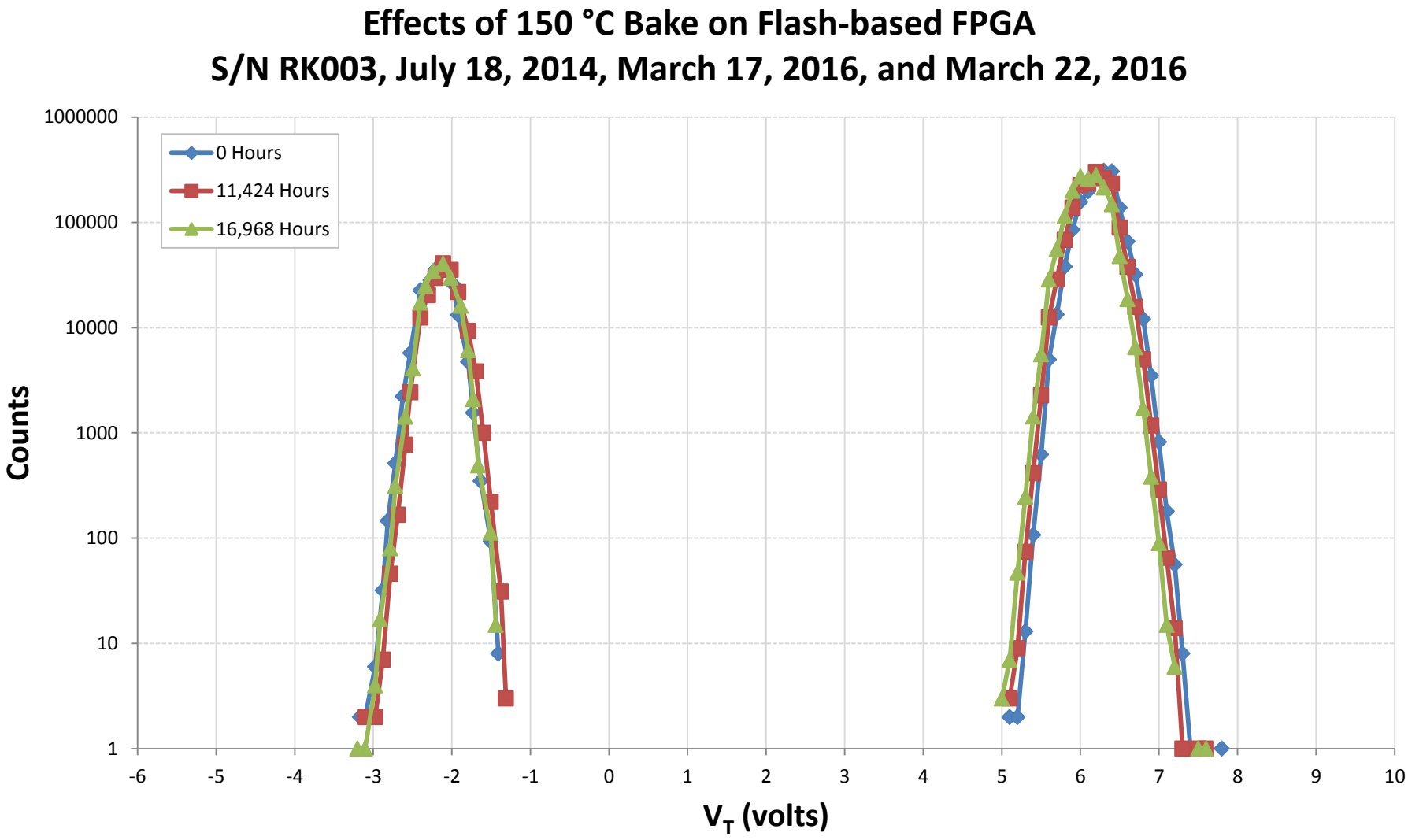
Tj (°C)	Spec Life (years)	6,000 Hour Data Life (years)
70	102.7	306.8
85	43.8	131.1
100	20.0	60.0
105	15.6	46.9
110	12.3	36.9
115	9.7	29.2
120	7.7	23.2
125	6.2	18.6
130	5.0	15.0
135	4.0	12.1
140	3.3	9.8
145	2.7	8.0
150	2.2	6.6

Specification Data From RT and Military ProASIC3 Data Sheets.

6,000 Hour Data derived predictions courtesy of Microsemi Corporation.


A3P250L FPGA Average Erased V_T
16,968 Hours @ 150 °C, March 21, 2017
Average V_T
-1.9
-2.0
-2.1
-2.2
-2.3
-2.4
-2.5
0
100
200
300
400
500
600
700
800
Time (Days)
S/N CK002
S/N CK003
S/N RK002
S/N RK003


A3P250L FPGA Average Programmed V_T
16,968 Hours @ 150 °C, March 21, 2017
S/N CK002
S/N CK003
S/N RK002
S/N RK003
Average V_T(volts)
7.0
6.9
6.8
6.7
6.6
6.5
6.4
6.3
6.2
6.1
6.0
0
100
200
300
400
500
600
700
800
Time (Days)


Effects of 150 °C Bake on Flash-based FPGA
S/N RK003, July 18, 2014, March 17, 2016, and March 22, 2016
0 Hours
11,424 Hours
16,968 Hours
Counts
1000000
100000
10000
1000
100
10
1
-6
-5
-4
-3
-2
-1
0
1
2
3
4
5
6
7
8
9
10
V_T (volts)

A3PL FPGA Flash Cell Data ESD Experiment

ESD Experiment Description

Family:	Microsemi A3PL
Model:	A3P250L
Lot:	QLWY8
Quantity:	40
Temp:	25 °C
Tests:	Phase Lock Loop (PLL): 500 V
	Other Power and I/O: 2kV
Date:	2016, Two Rounds
Facility:	DMEA Thermo Scientific MK. 1 ESD and Static Latch-up Test System

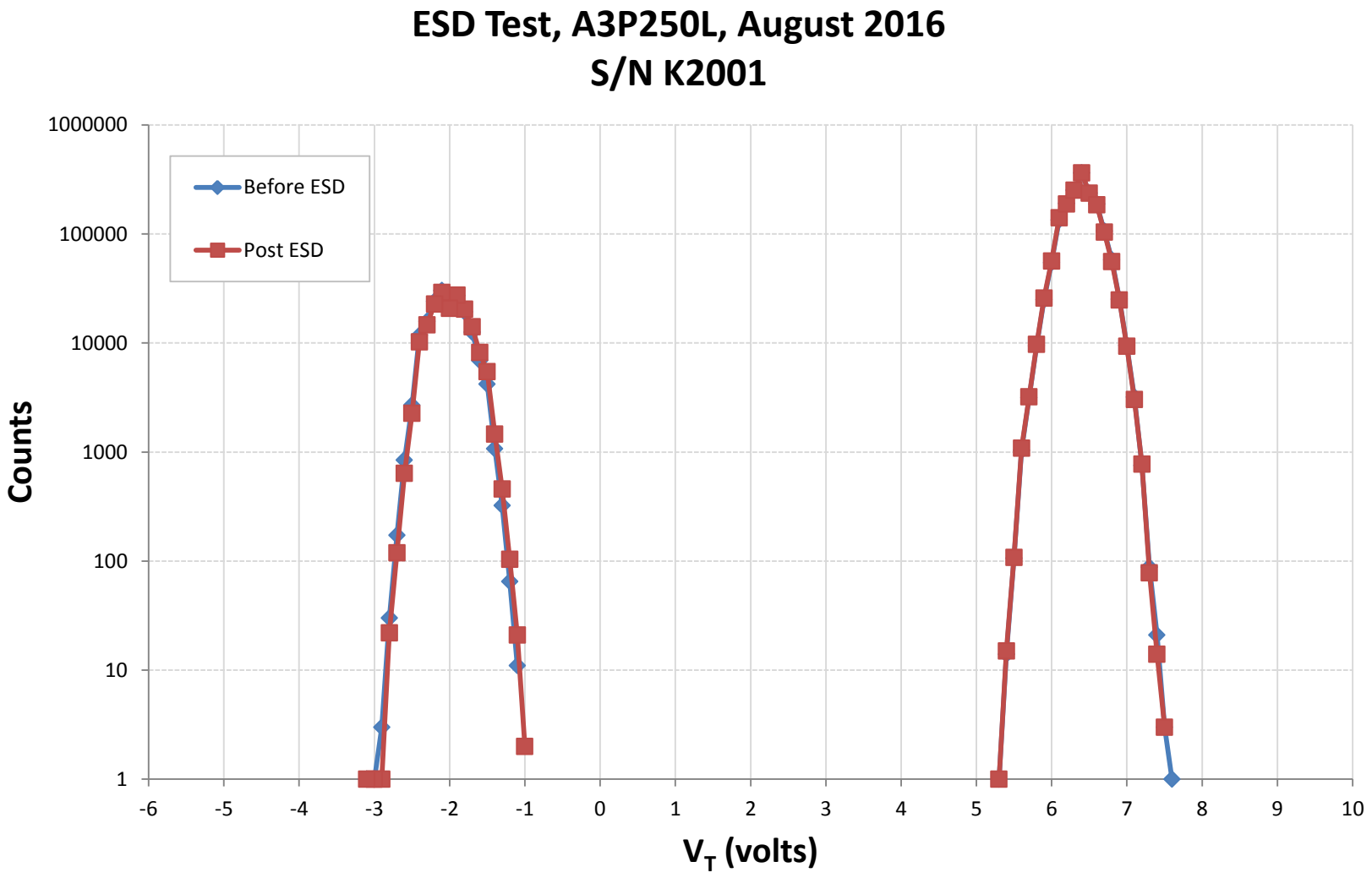
ESD Test Result Summary

- Testing done with 20 parts in 3 groups + controls
  - PLL (500V), Configuration Pins (2000V), I/O (2,000 V)

- Round 1, July 14, 2016
  - Test Error: 2,000 V applied to all pins
  - Two DUTs failure (appears non-flash related; awaiting failure analysis)
  - All other parts: no change in V_{TH} histograms

- Round 2, September 7, 2016
  - No failures
  - No change in V_{TH} histograms

Typical ESD Test Histograms

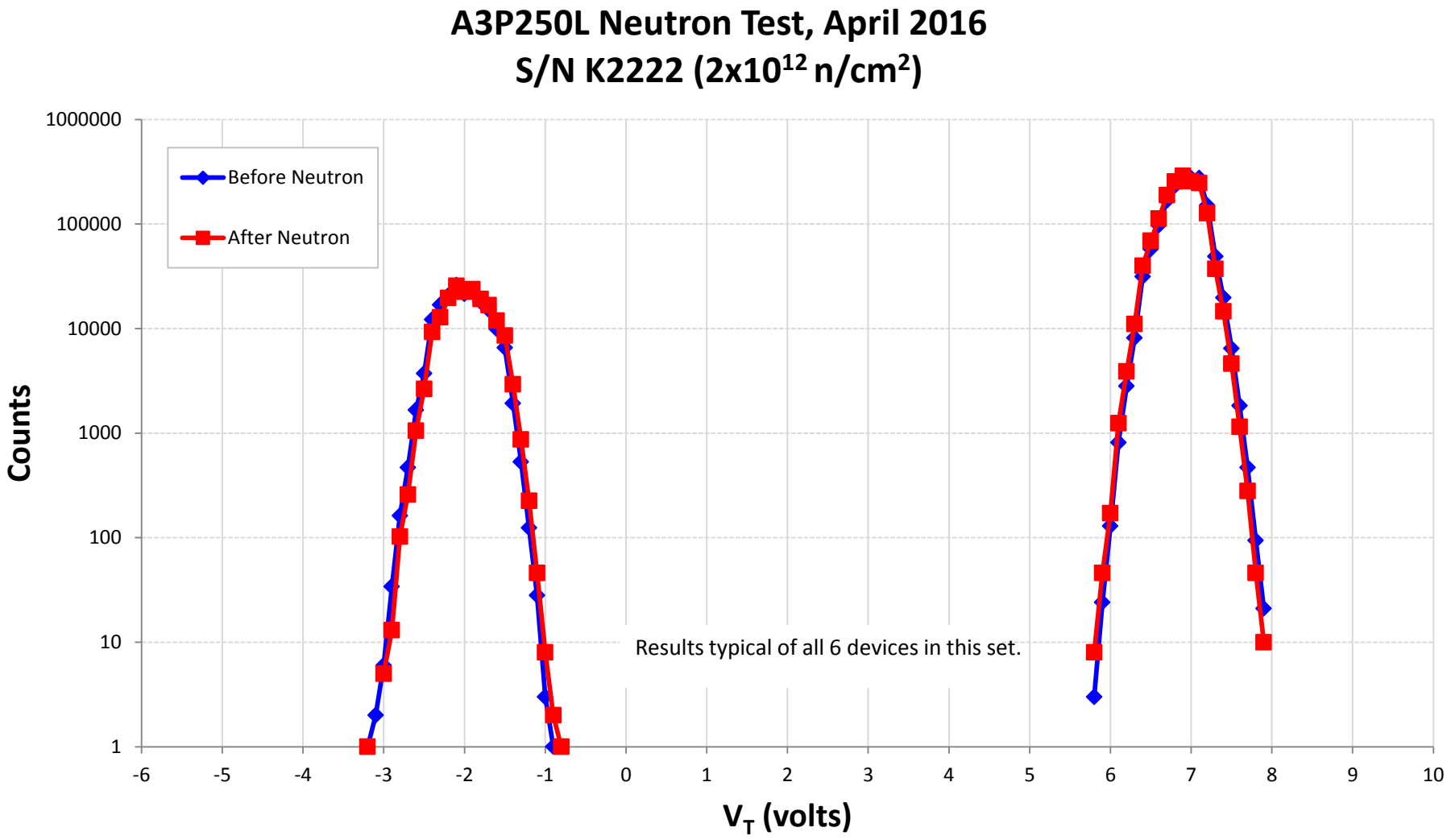


A3PL FPGA Flash Cell Data Neutron Dose Experiment

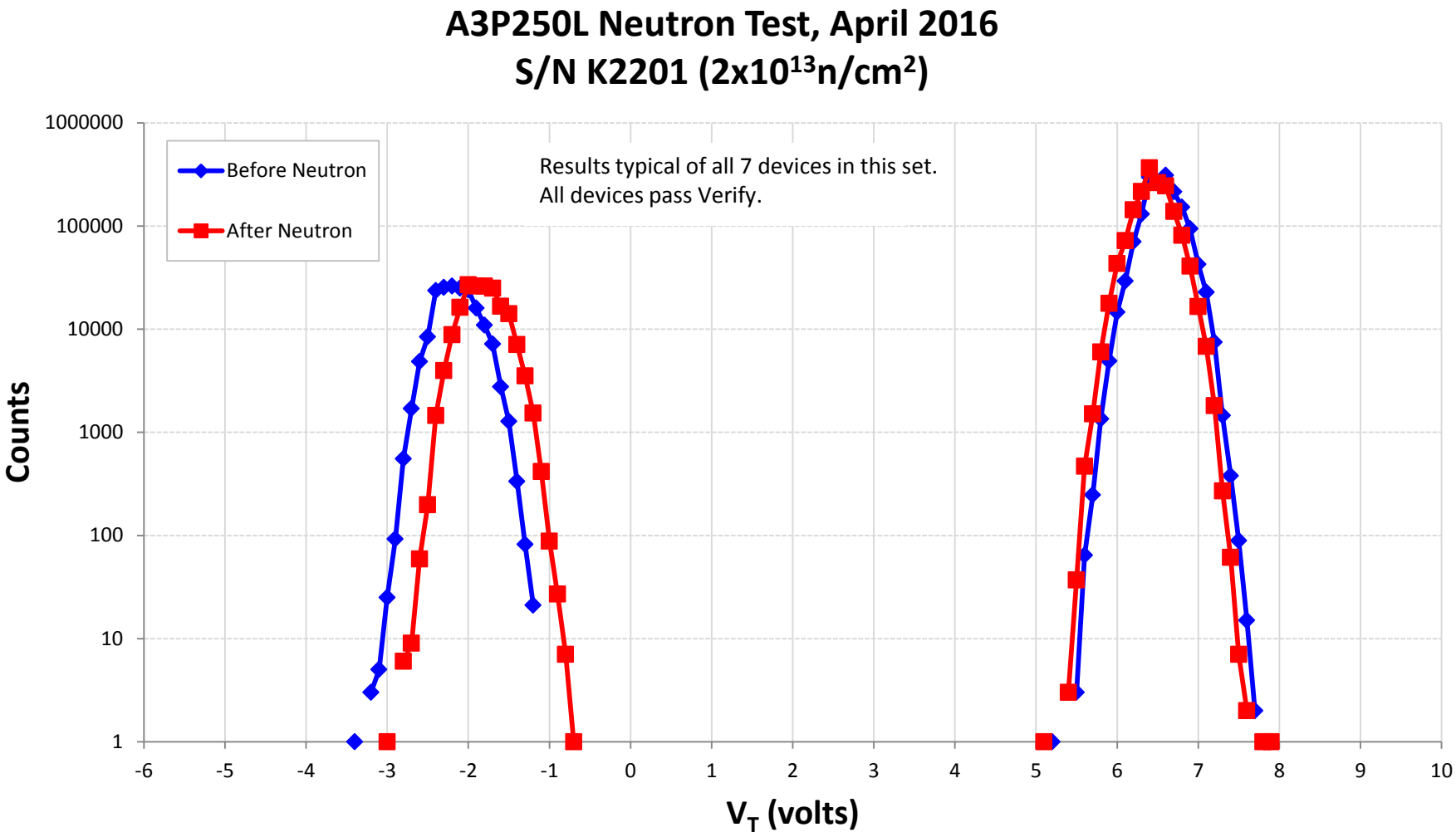
Neutron Dose Experiment Description

Family:	Microsemi A3PL
Model:	A3P250L
Lot:	QLWY8
Quantity:	20
Temp:	25 °C
Tests:	2×10^{12} n/cm^2 (7 DUTs)
	2×10^{13} n/cm^2 (7 DUTs)
	2×10^{14} n/cm^2 (6 DUTs)
Date:	April 2016
Facility:	McClellan Nuclear Research Center

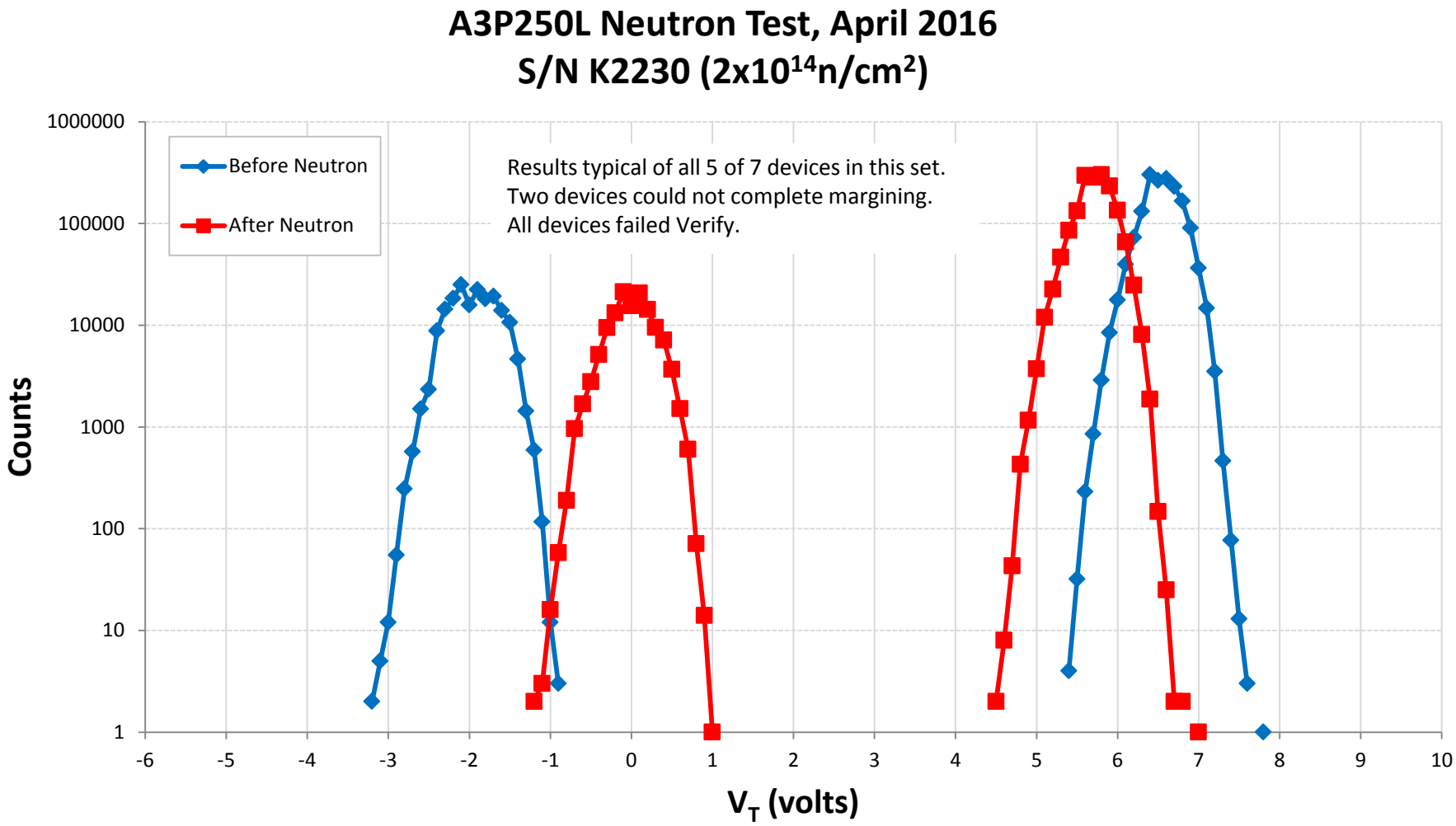
Neutron Testing: 2 x 10^{12} n/cm^2



Neutron Testing: 2 x 10^{13} n/cm^2



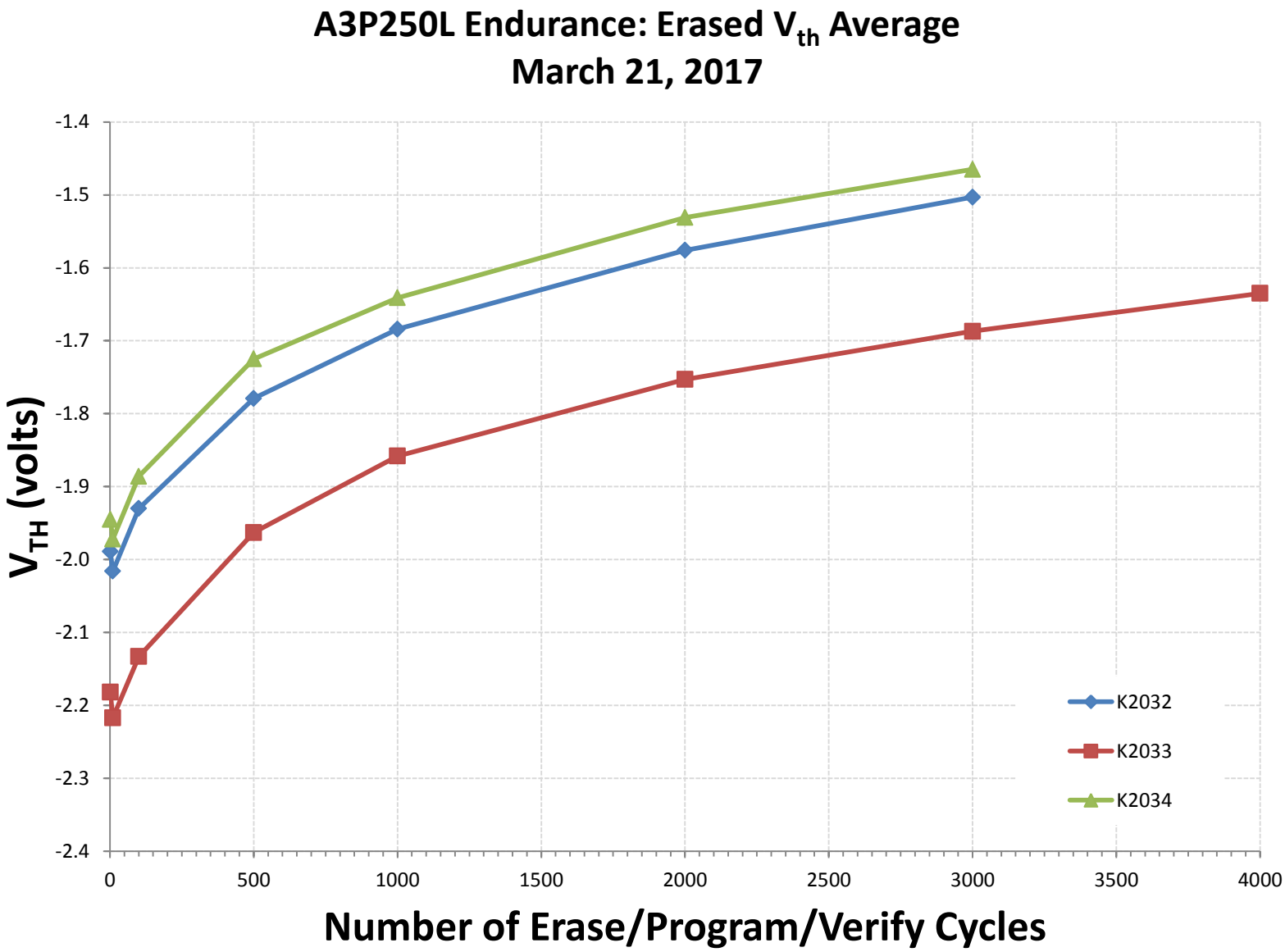
Neutron Testing: 2 x 10^{14} n/cm^2

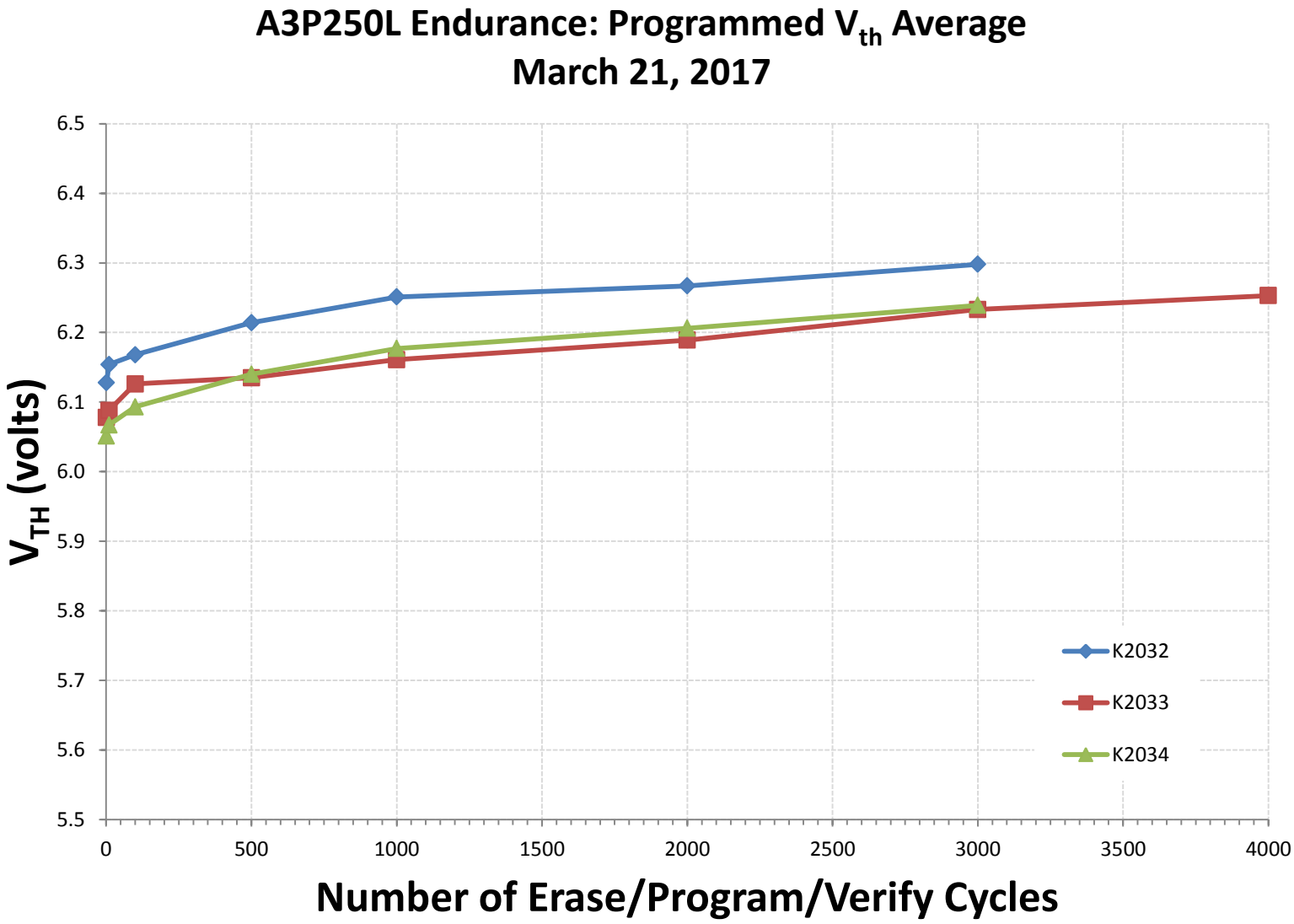


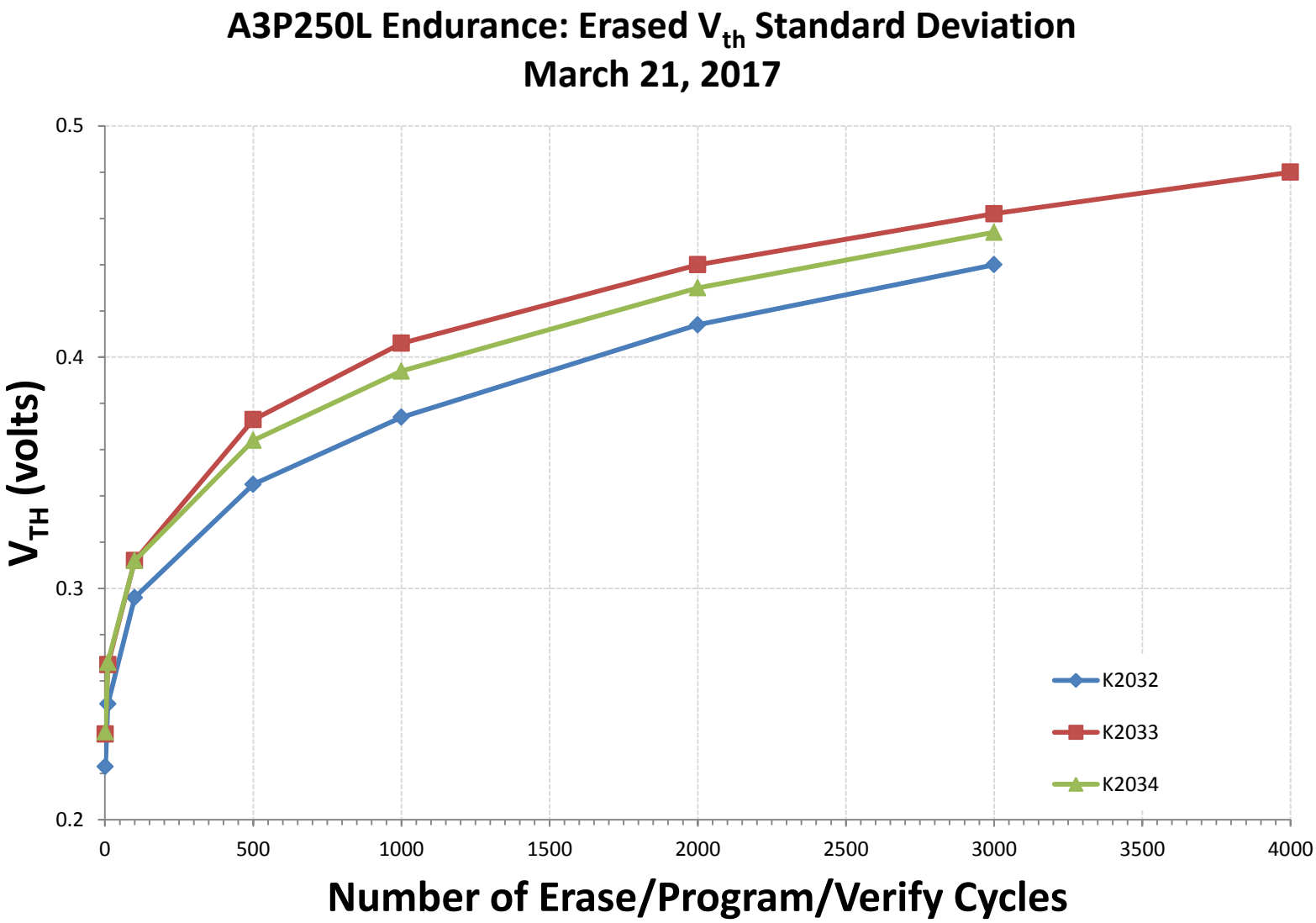
A3PL FPGA Flash Cell Data Endurance Experiment

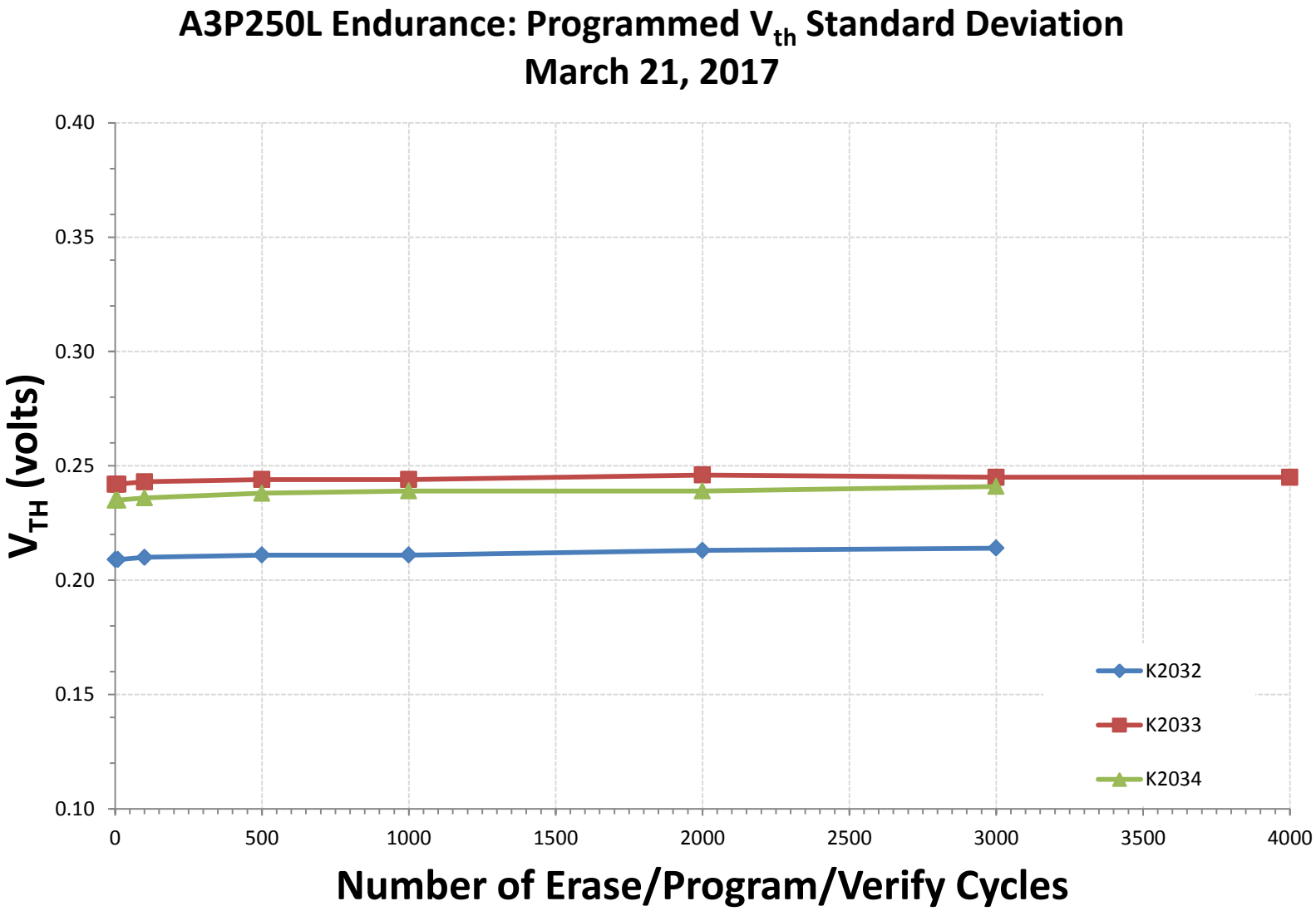
A3PL Endurance Experiment Description

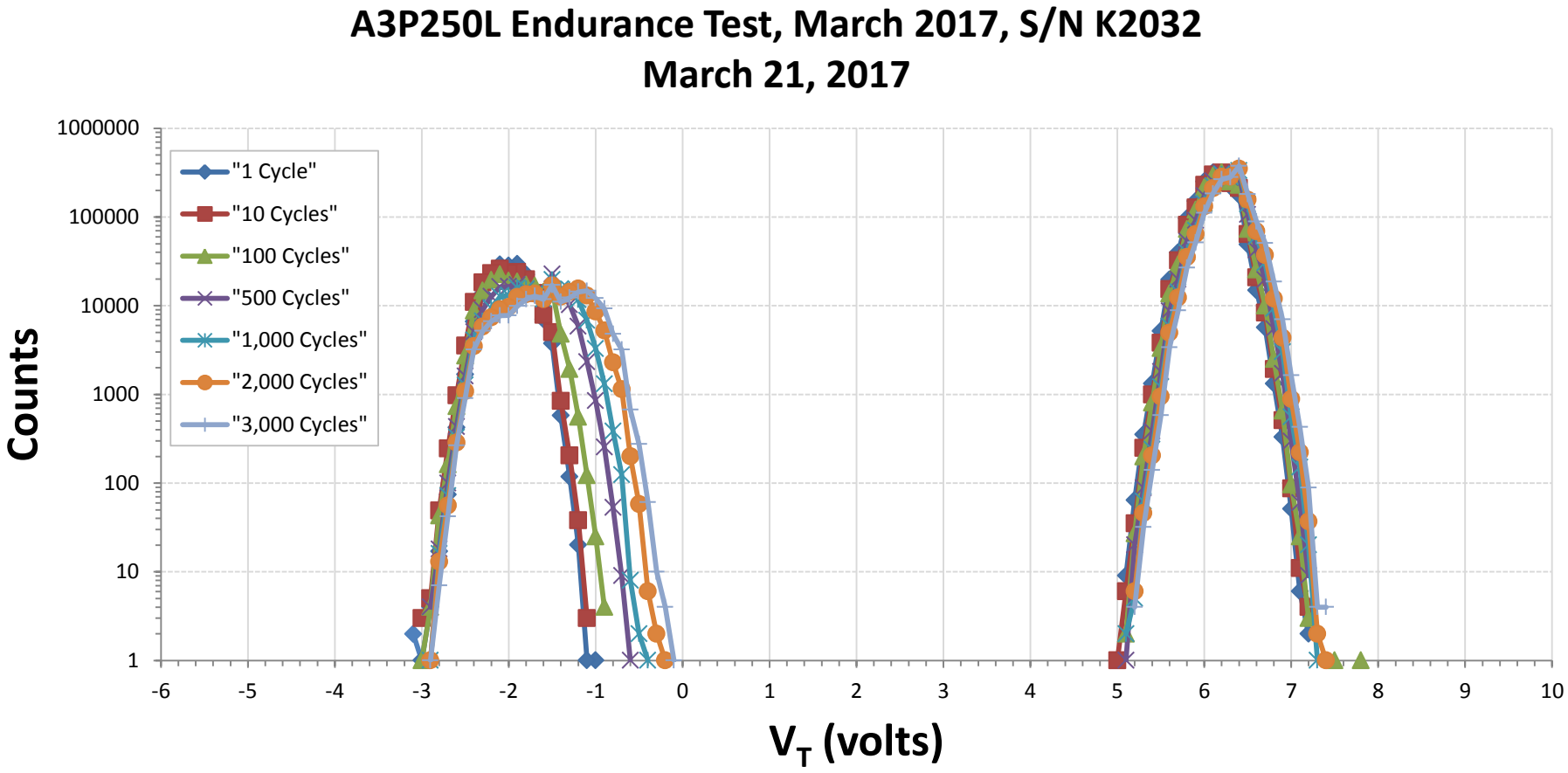
Family:	Microsemi A3PL
Model:	A3P250L
Lot:	QLWY8
Quantity:	3
Pattern:	9 unique patterns (unchanged)
Temp:	25 °C
Tests:	“Verify” each erase/program cycle
	Margin at key steps
Start:	March 3, 2017

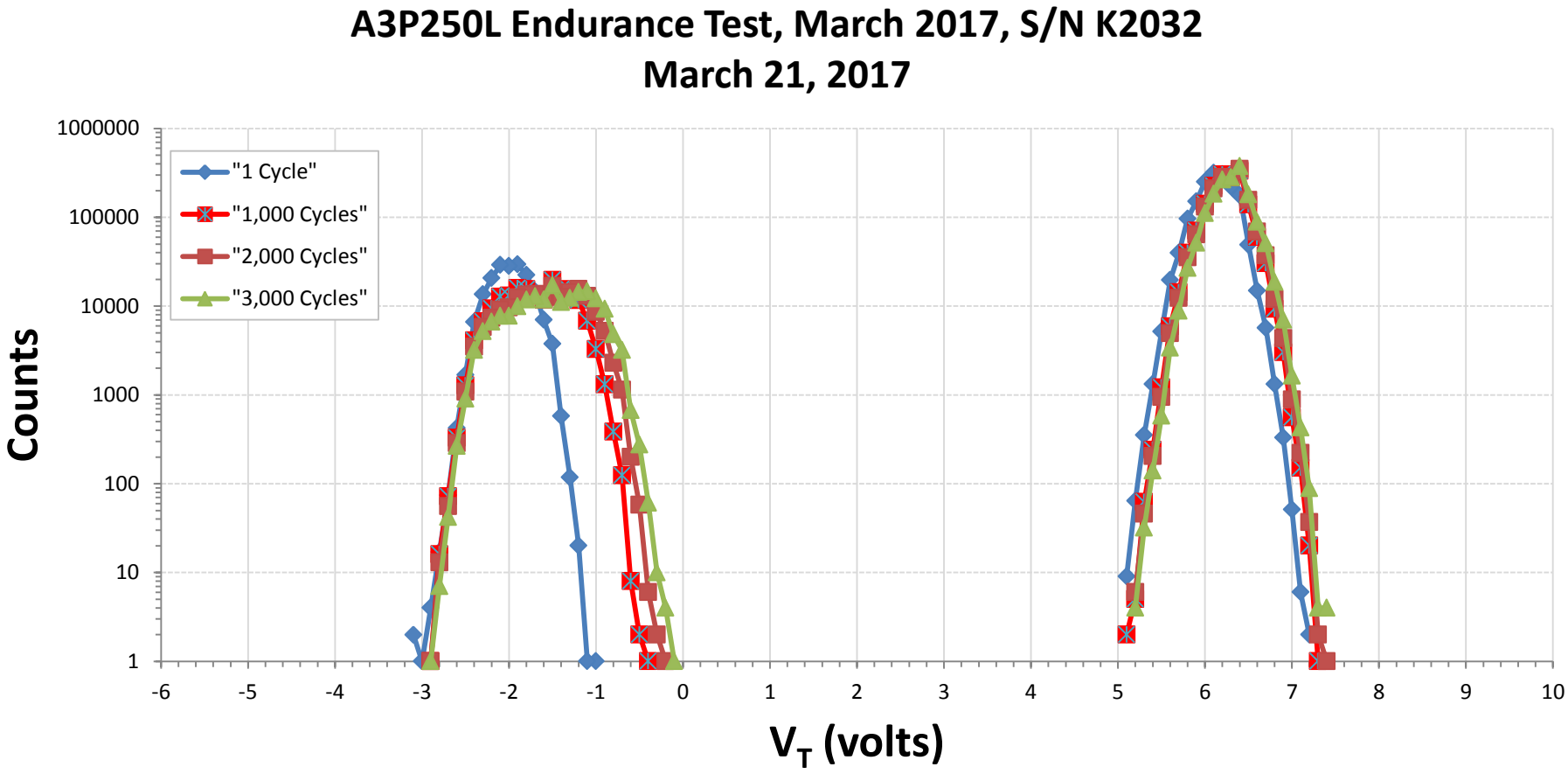

A3P250L Endurance: Erased V_{th} Average
March 21, 2017
V_{TH} (volts)
-1.4
-1.5
-1.6
-1.7
-1.8
-1.9
-2.0
-2.1
-2.2
-2.3
-2.4
0
500
1000
1500
2000
2500
3000
3500
4000
Number of Erase/Program/Verify Cycles
K2032
K2033
K2034

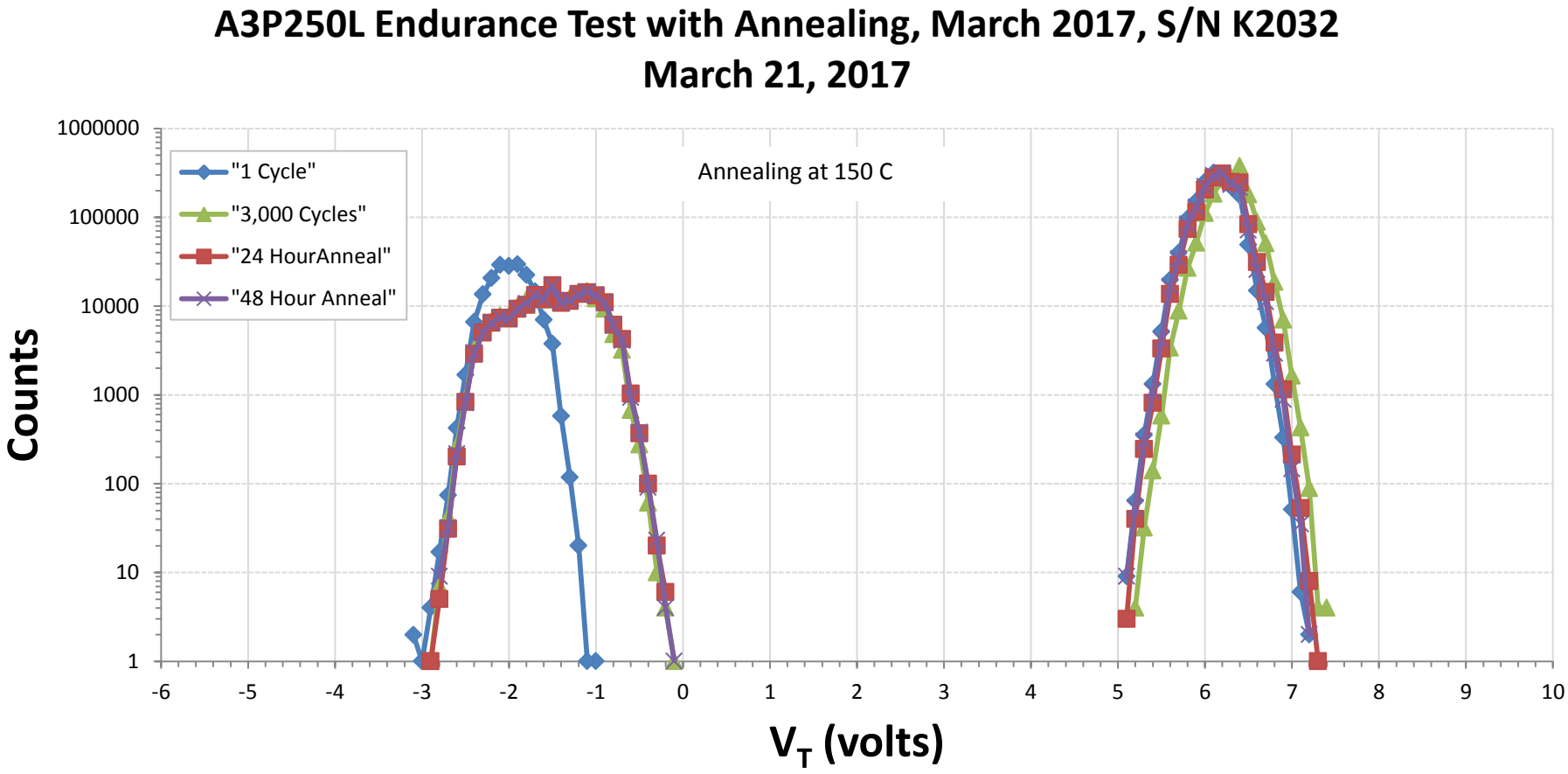

A3P250L Endurance: Programmed V_{th} Average
March 21, 2017
V_{TH} (volts)
6.5
6.4
6.3
6.2
6.1
6.0
5.9
5.8
5.7
5.6
5.5
0
500
1000
1500
2000
2500
3000
3500
4000
Number of Erase/Program/Verify Cycles
K2032
K2033
K2034


A3P250L Endurance: Erased V_{th} Standard Deviation
March 21, 2017
V_{TH} (volts)
0.5
0.4
0.3
0.2
0
500
1000
1500
2000
2500
3000
3500
4000
Number of Erase/Program/Verify Cycles
K2032
K2033
K2034


A3P250L Endurance: Programmed V_{th} Standard Deviation
March 21, 2017
V_{TH} (volts)
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0
500
1000
1500
2000
2500
3000
3500
4000
Number of Erase/Program/Verify Cycles
K2032
K2033
K2034


A3P250L Endurance Test, March 2017, S/N K2032
March 21, 2017
Counts
1000000
100000
10000
1000
100
10
1
"1 Cycle"
"10 Cycles"
"100 Cycles"
"500 Cycles"
"1,000 Cycles"
"2,000 Cycles"
"3,000 Cycles"
-6
-5
-4
-3
-2
-1
0
1
2
3
4
5
6
7
8
9
10
V_T (volts)


A3P250L Endurance Test, March 2017, S/N K2032
March 21, 2017
Counts
1000000
100000
10000
1000
100
10
1
"1 Cycle"
"1,000 Cycles"
"2,000 Cycles"
"3,000 Cycles"
-6
-5
-4
-3
-2
-1
0
1
2
3
4
5
6
7
8
9
10
V_T (volts)


A3P250L Endurance Test with Annealing, March 2017, S/N K2032
March 21, 2017
Annealing at 150 C
"1 Cycle"
"3,000 Cycles"
"24 HourAnneal"
"48 Hour Anneal"
Counts
1000000
100000
10000
1000
100
10
1
-6
-5
-4
-3
-2
-1
0
1
2
3
4
5
6
7
8
9
10
V_T (volts)

Large Population Temperature Testing

Temperature Experiment Summary

Large Population

- **# of DUTs: 1,008 (excluding control DUTs)**
- **# of Outliers[1]: 7 (~0.7%)**
- **# of Part Failures[2]: 1**

[1]All outliers were erased cells and passed Verify test.

[2]K1631 would not margin or verify; likely non-flash failure, under failure analysis. All other DUTs passed.

Roster of Parts

	25 °C	125 °C	150 °C
Lot F	24	12	8
Lot K	365	299	300
Totals	**389**	**311**	**308**

Population: Average Data and Analysis

Lot K

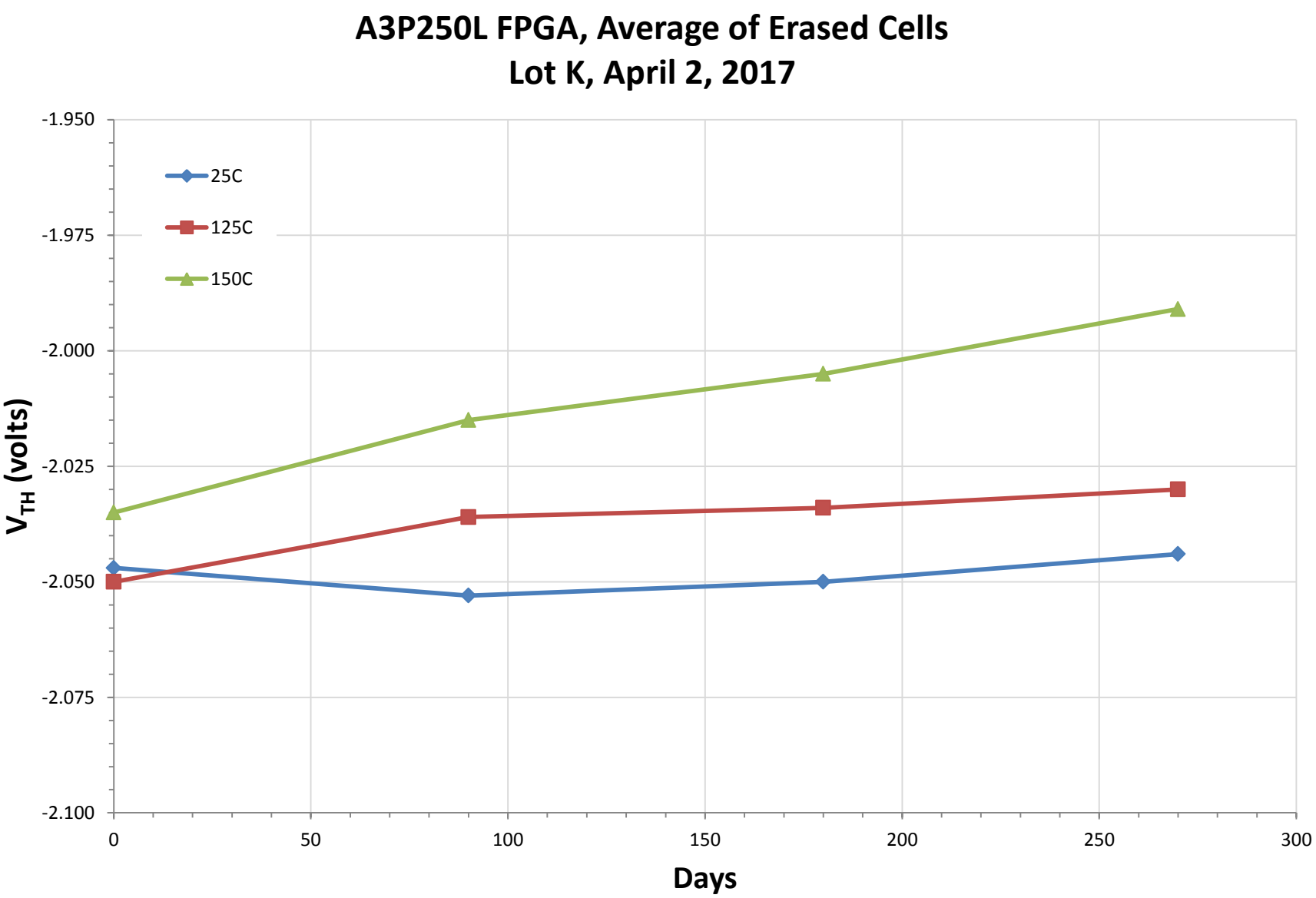
# Days	Avg Erase 25 °C	Avg Erase 125 °C	Avg Erase 150 °C
0	-2.047	-2.050	-2.035
90	-2.053	-2.036	-2.015
180	-2.050	-2.034	-2.005
270	-2.044	-2.030	-1.991

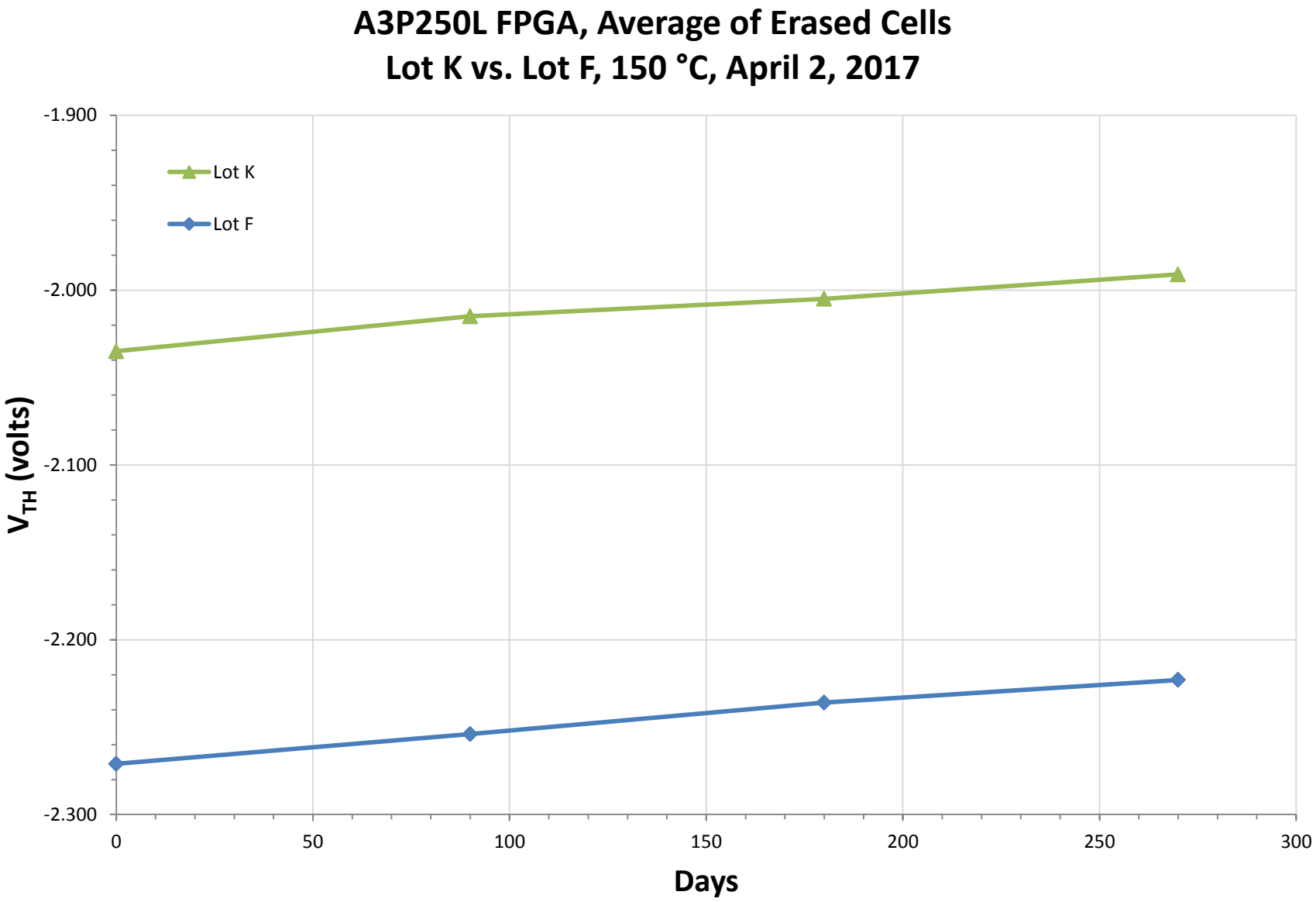
# Days	Avg Program 25 °C	Avg Program 125 °C	Avg Program 150 °C
0	6.284	6.301	6.249
90	6.268	6.245	6.161
180	6.269	6.237	6.162
270	6.274	6.235	6.171

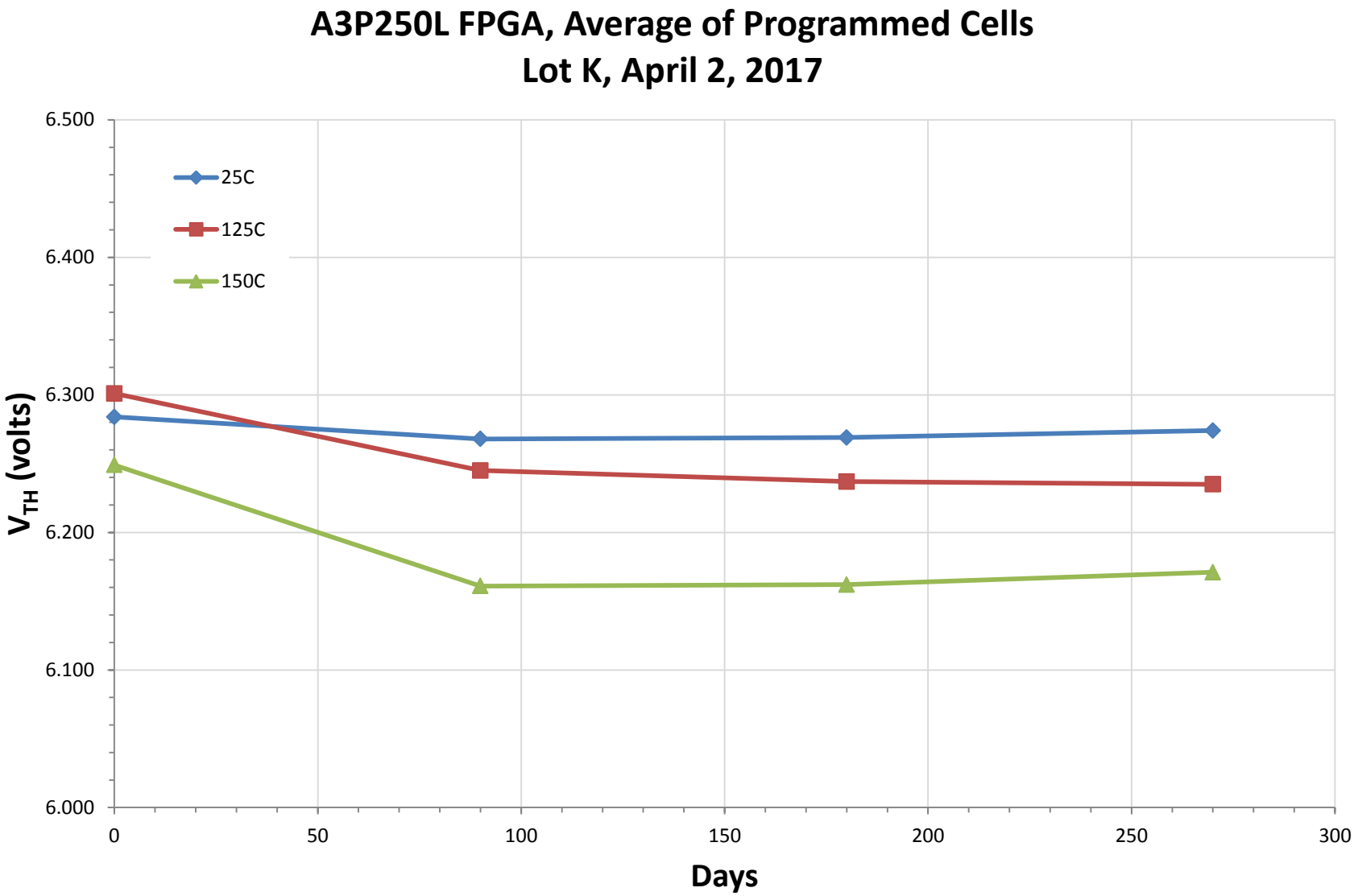
Lot F

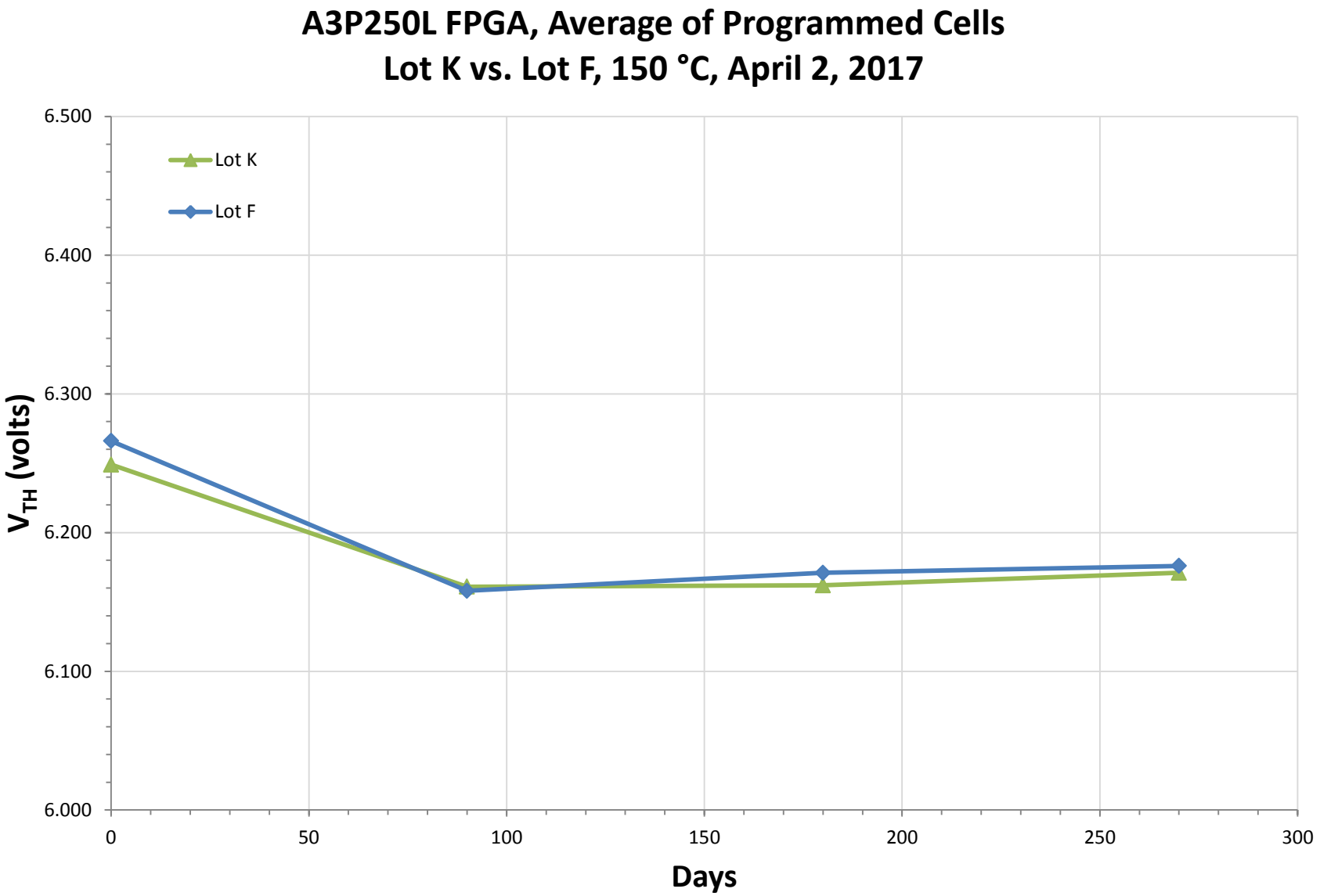
# Days	Avg Erase 25 °C	Avg Erase 125 °C	Avg Erase 150 °C
0	-2.258	-2.342	-2.271
90	-2.268	-2.323	-2.254
180	-2.262	-2.328	-2.236
270	-2.255	-2.319	-2.223

# Days	Avg Program 25 °C	Avg Program 125 °C	Avg Program 150 °C
0	6.298	6.379	6.266
90	6.274	6.319	6.158
180	6.278	6.304	6.171
270	6.286	6.303	6.176


A3P250L FPGA, Average of Erased Cells
Lot K, April 2, 2017
-1.950
-1.975
-2.000
-2.025
-2.050
-2.075
-2.100
25C
125C
150C
V_{TH} (volts)
0
50
100
150
200
250
300
Days


A3P250L FPGA, Average of Erased Cells
Lot K vs. Lot F, 150 °C, April 2, 2017
-1.900
-2.000
-2.100
-2.200
-2.300
Lot K
Lot F
V_{TH} (volts)
0
50
100
150
200
250
300
Days


A3P250L FPGA, Average of Programmed Cells
Lot K, April 2, 2017
6.500
6.400
6.300
6.200
6.100
6.000
25C
125C
150C
V_{TH} (volts)
0
50
100
150
200
250
300
Days


A3P250L FPGA, Average of Programmed Cells
Lot K vs. Lot F, 150 °C, April 2, 2017
6.500
6.400
6.300
6.200
6.100
6.000
Lot K
Lot F
V_{TH} (volts)
0
50
100
150
200
250
300
Days

Population: Average (Standard Deviation) Data and Analysis

Lot K

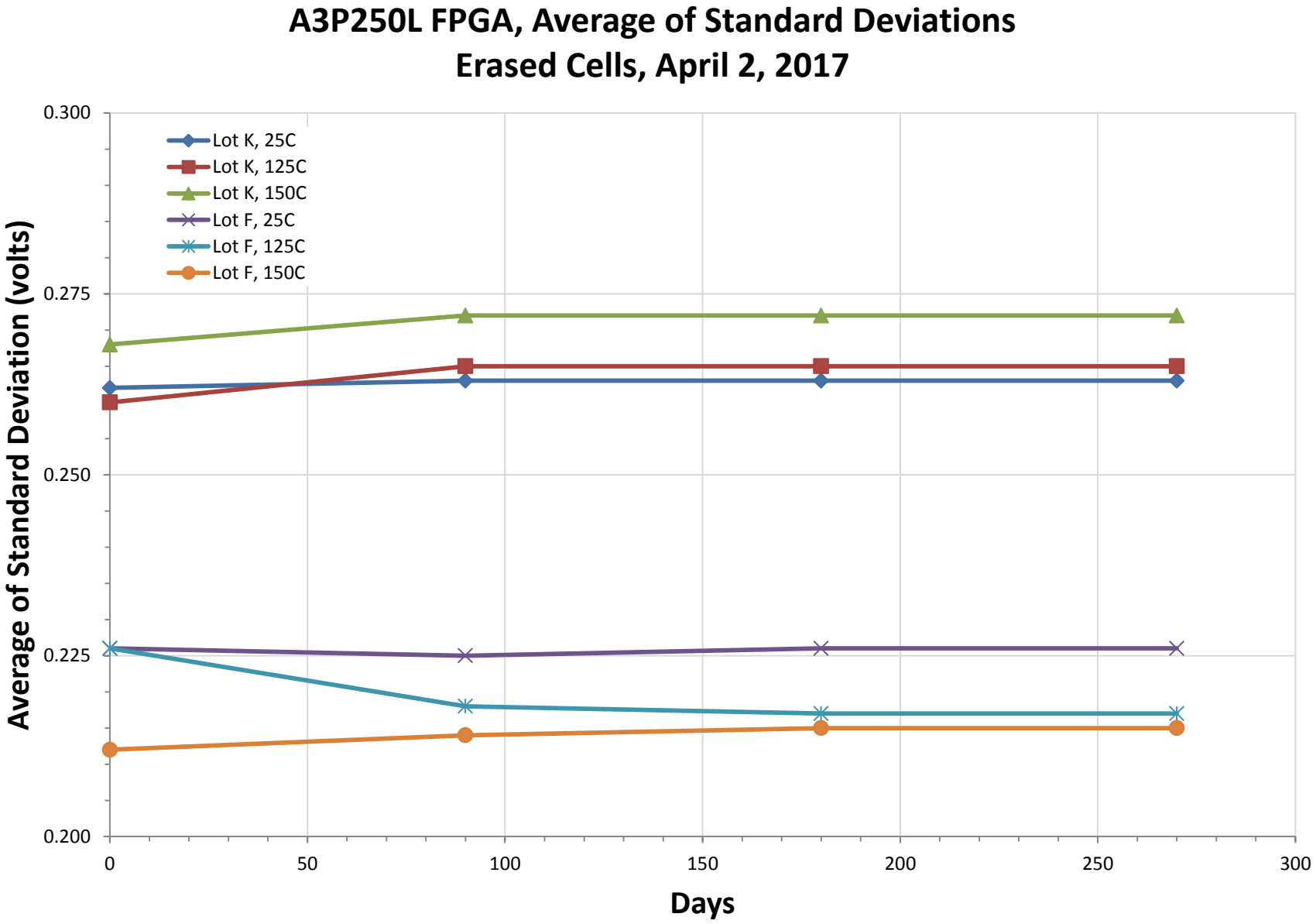
# Days	SD Erase 25 °C	Erase 125 °C	SD Erase 150 °C
0	0.262	0.260	0.268
90	0.263	0.265	0.272
180	0.263	0.265	0.272
270	0.263	0.265	0.272

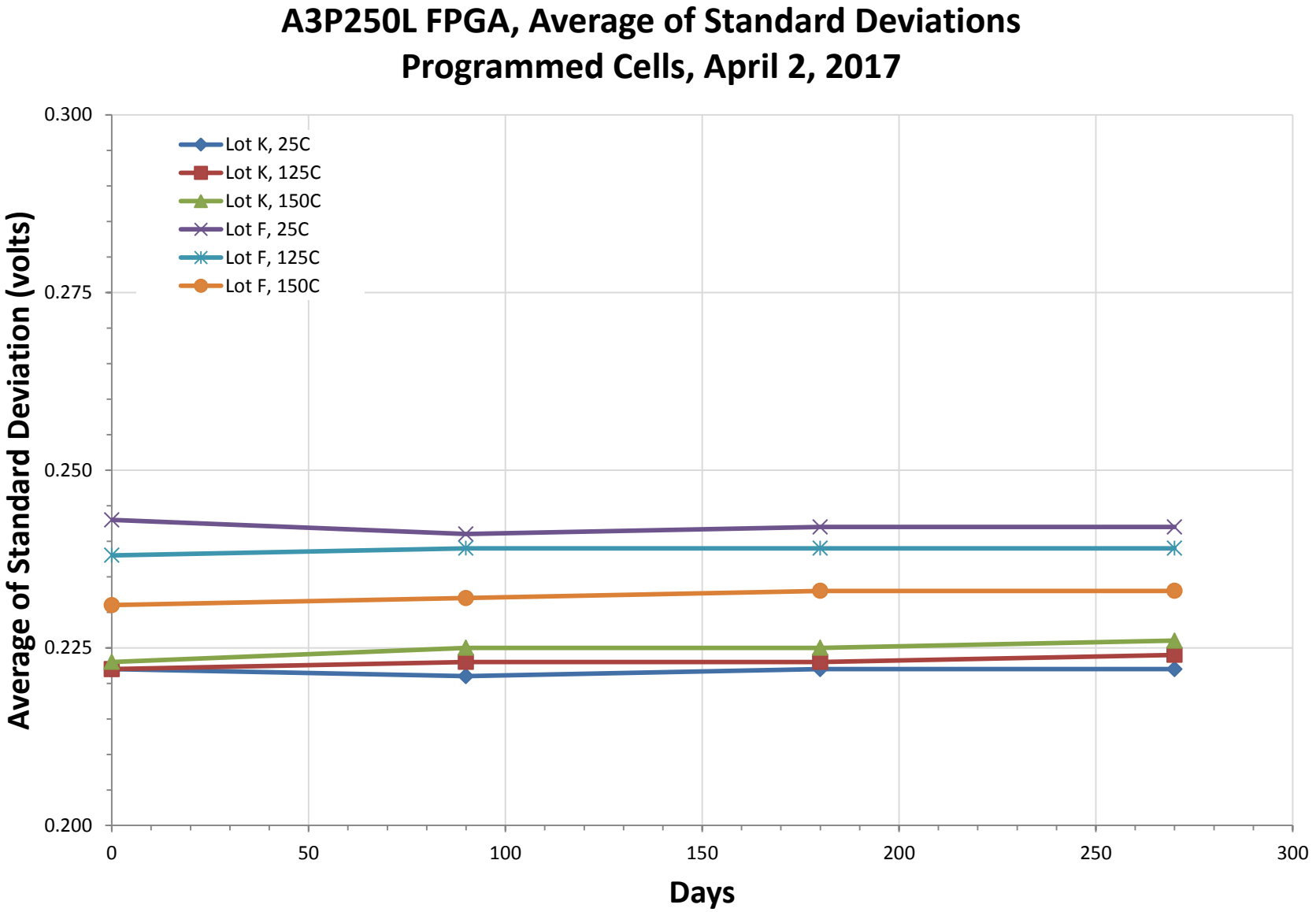
# Days	SD Program 25 °C	SD Program 125 °C	SD Program 150 °C
0	0.222	0.222	0.223
90	0.221	0.223	0.225
180	0.222	0.223	0.225
270	0.222	0.224	0.226

Lot F

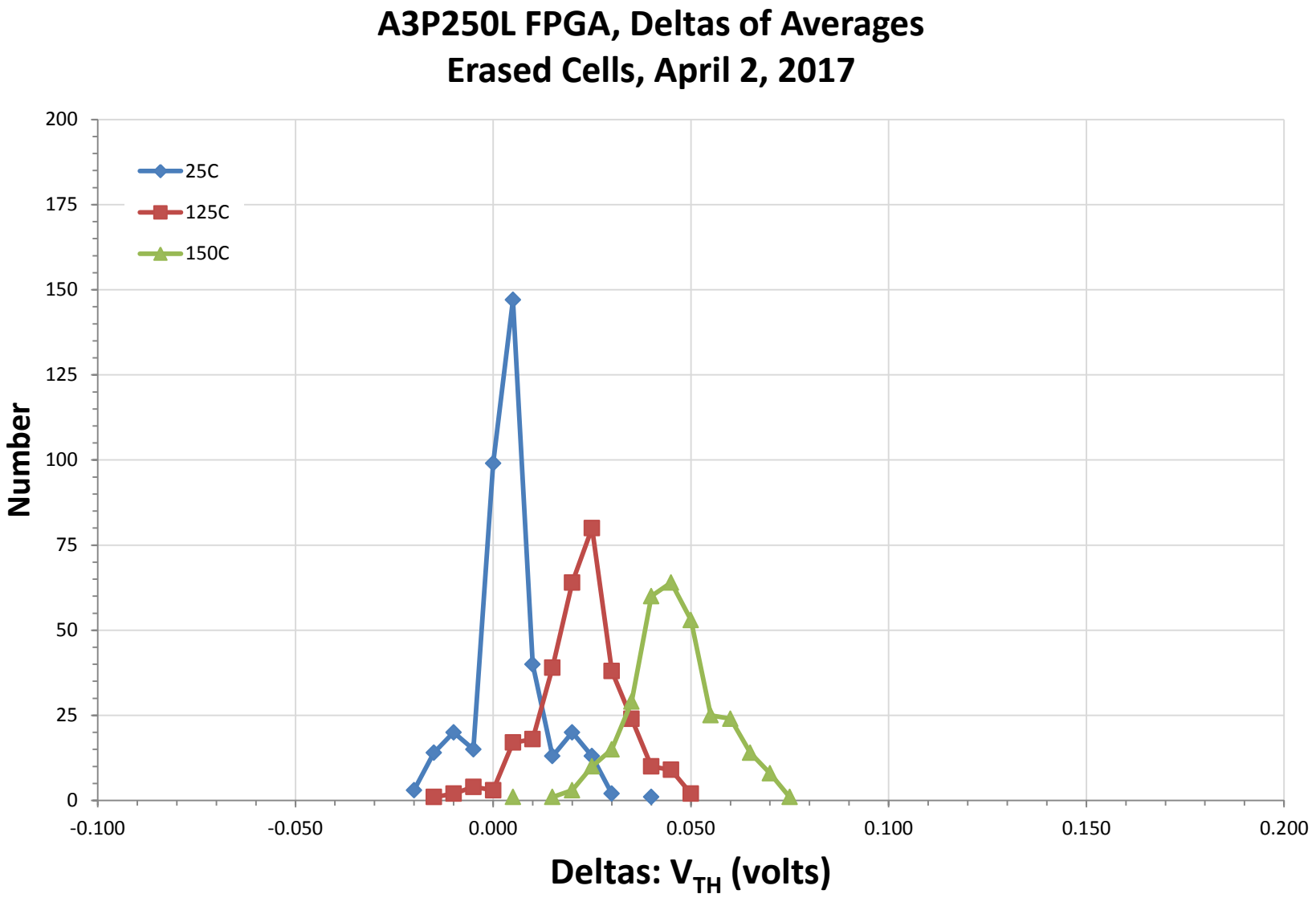
# Days	SD Erase 25 °C	SD Erase 125 °C	SD Erase 150 °C
0	0.226	0.226	0.212
90	0.225	0.218	0.214
180	0.226	0.217	0.215
270	0.226	0.217	0.215

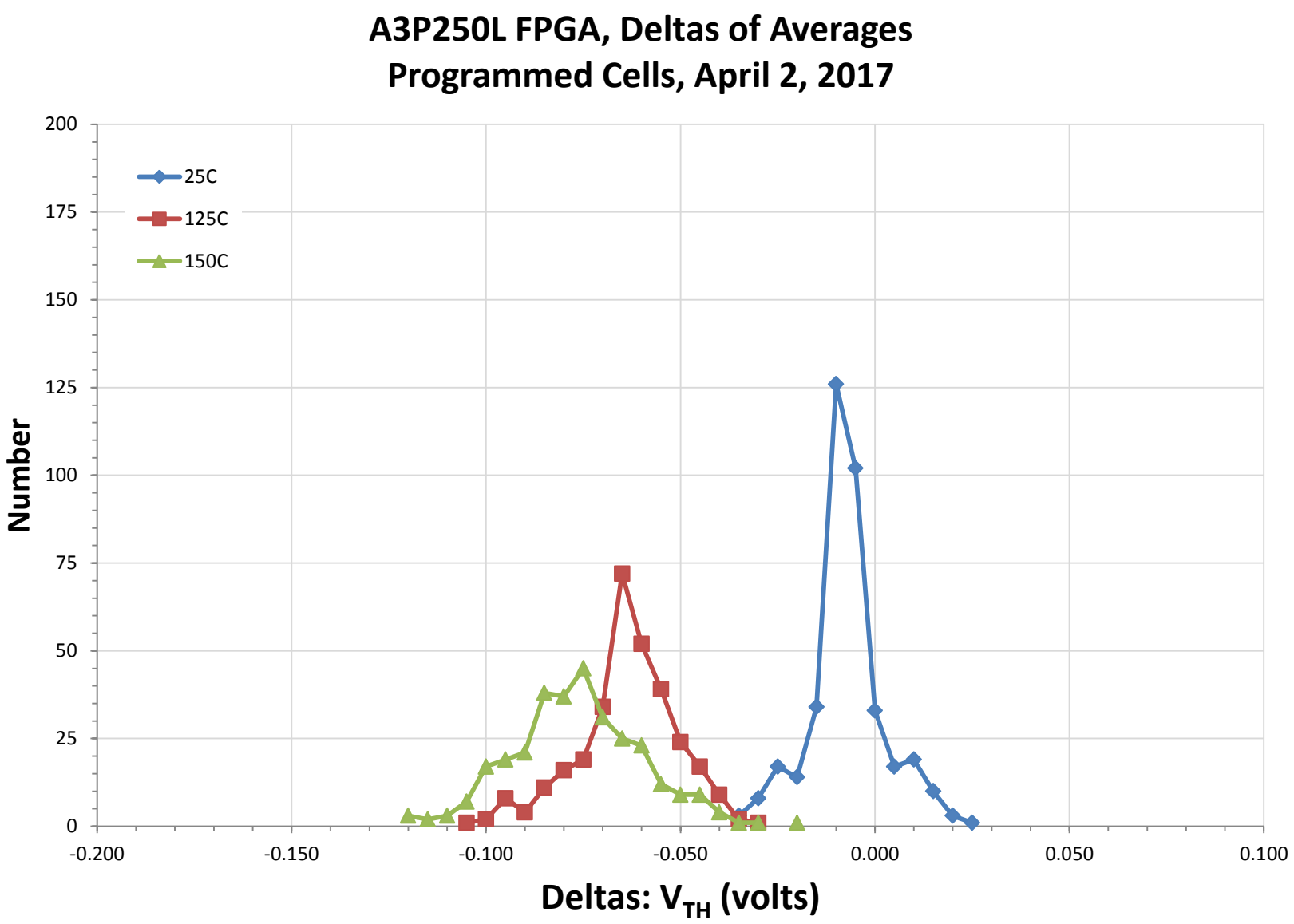
# Days	SD Program 25 °C	SD Program 125 °C	SD Program 150 °C
0	0.243	0.238	0.231
90	0.241	0.239	0.232
180	0.242	0.239	0.233
270	0.242	0.239	0.233

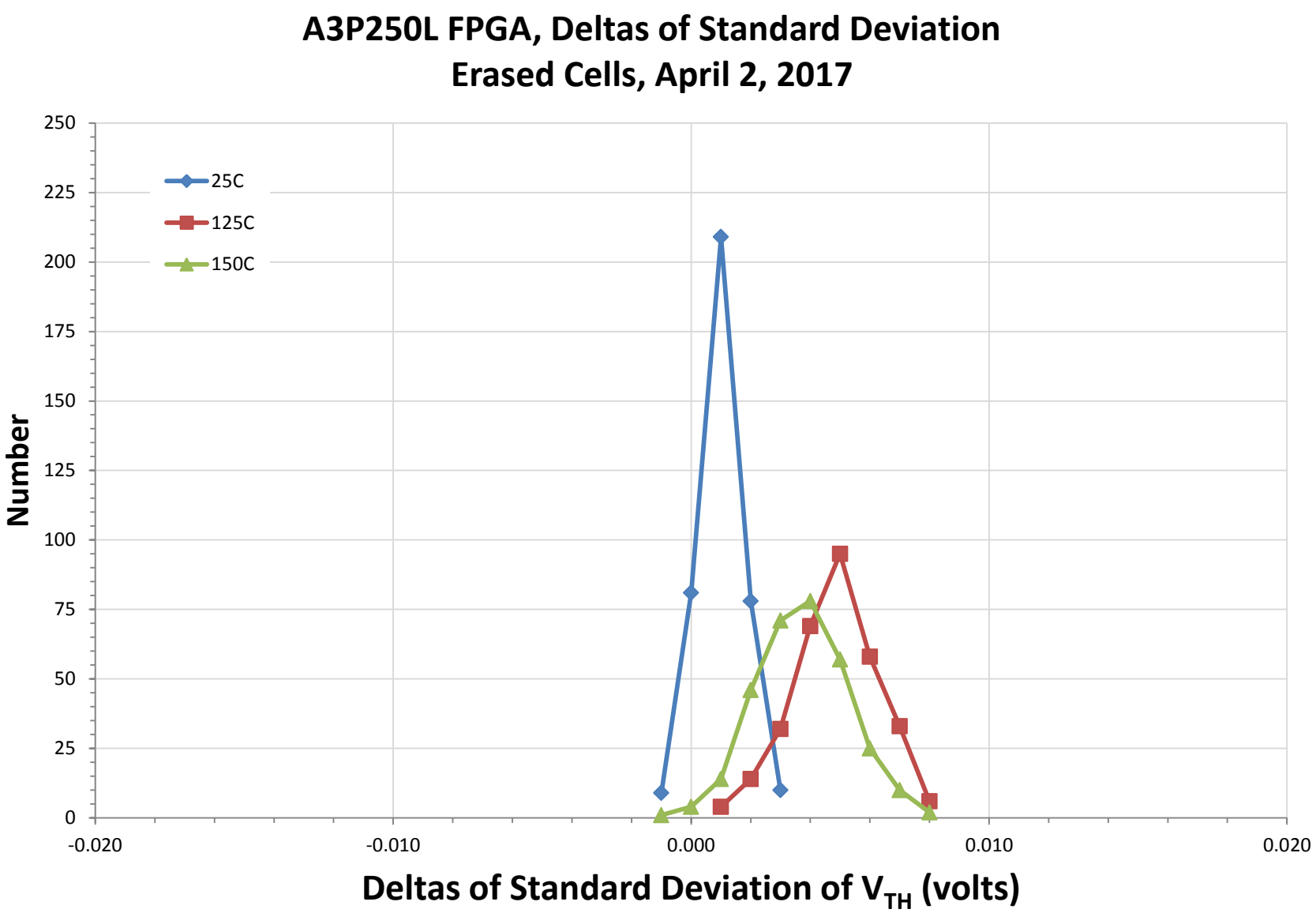

A3P250L FPGA, Average of Standard Deviations
Erased Cells, April 2, 2017
Average of Standard Deviation (volts)
0.300
0.275
0.250
0.225
0.200
Lot K, 25C
Lot K, 125C
Lot K, 150C
Lot F, 25C
Lot F, 125C
Lot F, 150C
0
50
100
150
200
250
300
Days

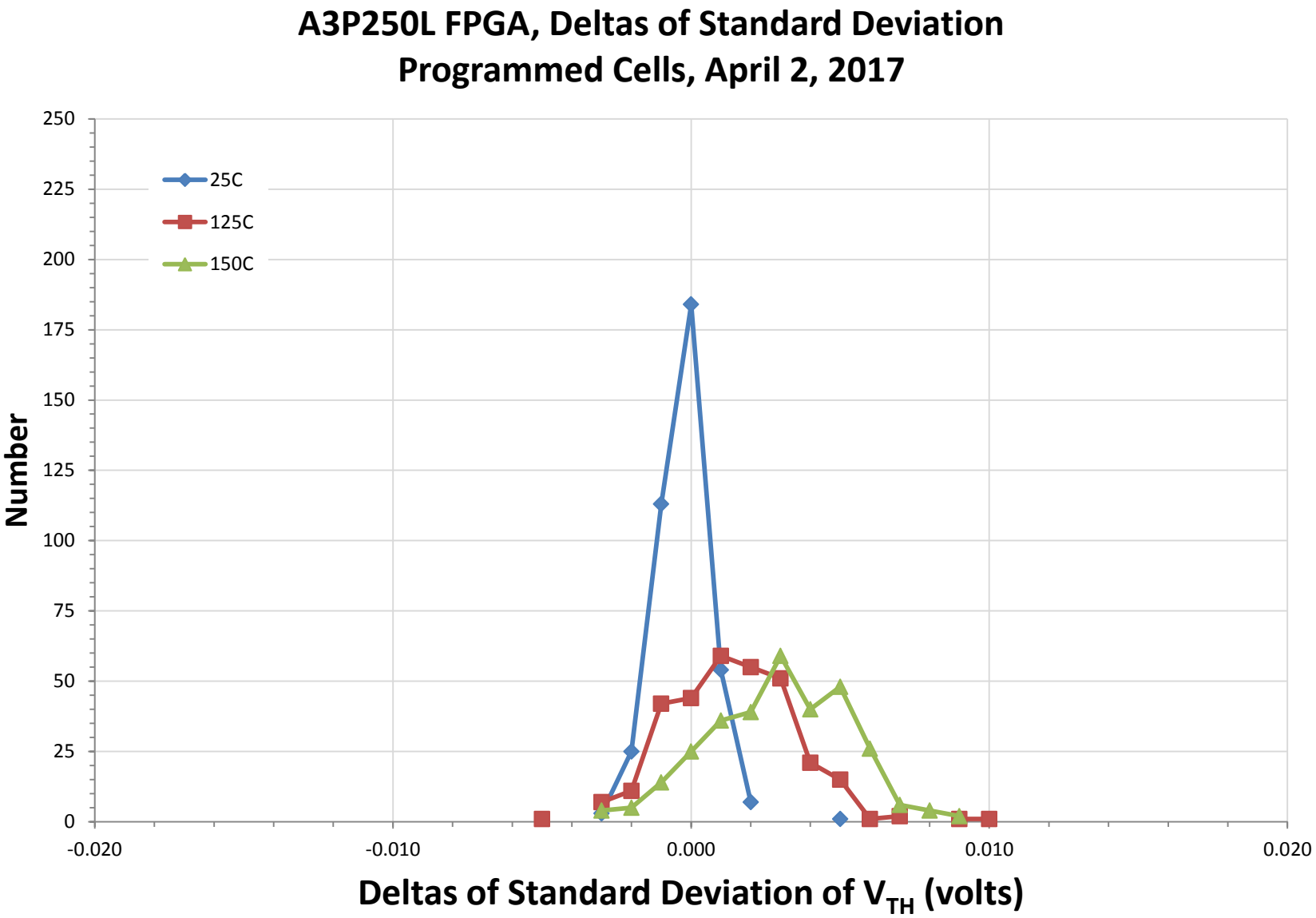

A3P250L FPGA, Average of Standard Deviations
Programmed Cells, April 2, 2017
Average of Standard Deviation (volts)
0.300
0.275
0.250
0.225
0.200
Lot K, 25C
Lot K, 125C
Lot K, 150C
Lot F, 25C
Lot F, 125C
Lot F, 150C
0
50
100
150
200
250
300
Days

Analyze Changes In Each DUT


A3P250L FPGA, Deltas of Averages
Erased Cells, April 2, 2017
25C
125C
150C
Number
200
175
150
125
100
75
50
25
0
-0.100
-0.050
0.000
0.050
0.100
0.150
0.200
Deltas: V_{TH} (volts)

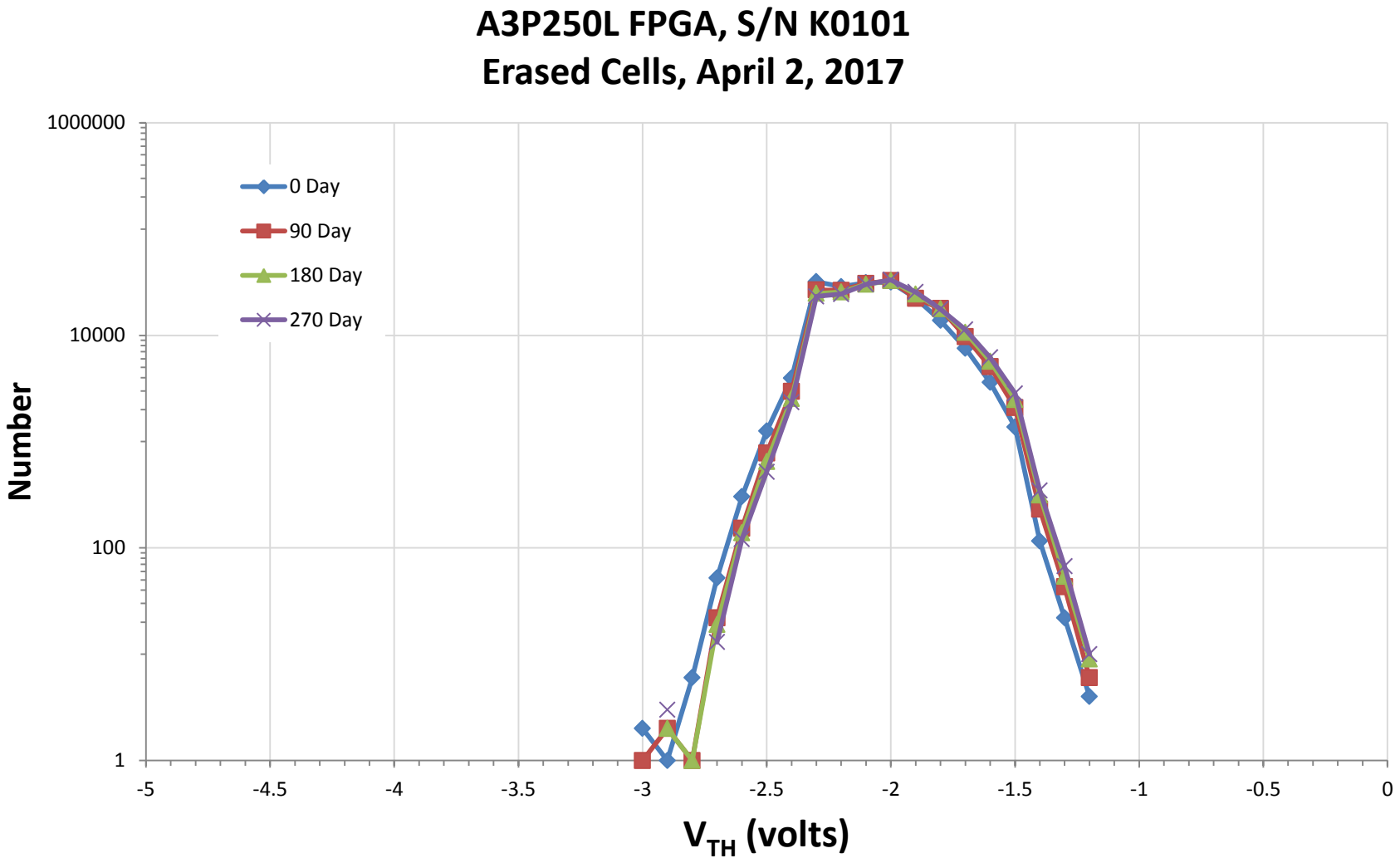

A3P250L FPGA, Deltas of Averages
Programmed Cells, April 2, 2017
25C
125C
150C
Number
200
175
150
125
100
75
50
25
0
-0.200
-0.150
-0.100
-0.050
0.000
0.050
0.100
Deltas: V_{TH} (volts)


A3P250L FPGA, Deltas of Standard Deviation
Erased Cells, April 2, 2017
25C
125C
150C
Number
250
225
200
175
150
125
100
75
50
25
0
-0.020
-0.010
0.000
0.010
0.020
Deltas of Standard Deviation of V_{TH} (volts)

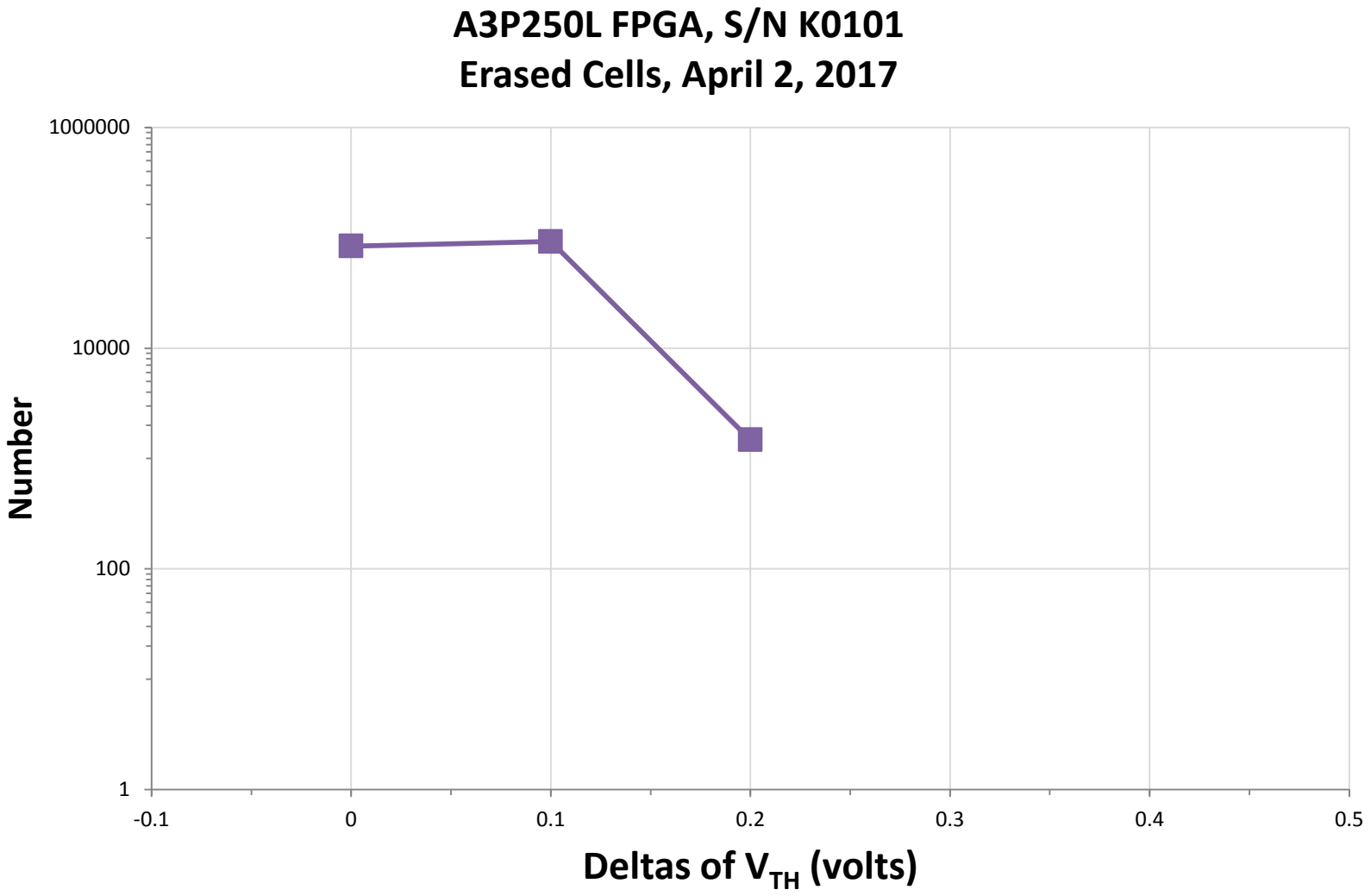

A3P250L FPGA, Deltas of Standard Deviation
Programmed Cells, April 2, 2017
25C
125C
150C
Number
250
225
200
175
150
125
100
75
50
25
0
-0.020
-0.010
0.000
0.010
0.020
Deltas of Standard Deviation of V_{TH} (volts)

Example of Delta Variation Within a DUT

Test History of S/N K0101



Sample: V_{TH} Change Within a DUT

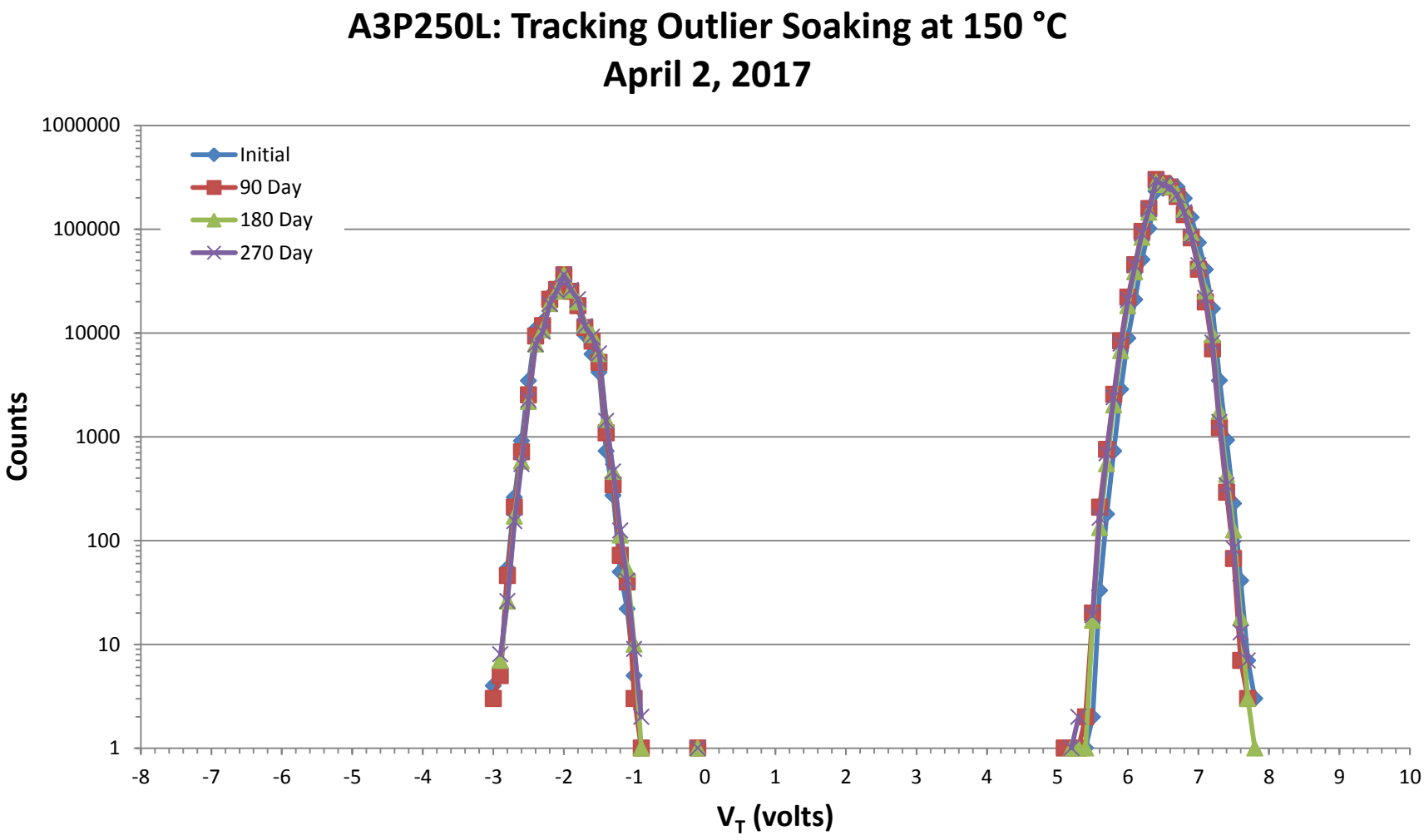


Outliers

Outliers

- Outlier population for A3P250L is ~ 1%
- Outliers distributed into 25 °C, 125 °C, and 150 °C groups.
- Each outlier is tracked and trended every 90 days both graphically and by examining data set.
- To date (270 days):
  - Outliers are stable.
  - No new outliers were detected.

Sample Outlier: Histogram



Sample Outlier: Data Set

Initial		90 Day		180 Day		270 Day	
0	0	0	0	0	0	0	0
-0.1	1	-0.1	1	-0.1	1	-0.1	1
-0.2	0	-0.2	0	-0.2	0	-0.2	0
-0.3	0	-0.3	0	-0.3	0	-0.3	0
-0.4	0	-0.4	0	-0.4	0	-0.4	0
-0.5	0	-0.5	0	-0.5	0	-0.5	0
-0.6	0	-0.6	0	-0.6	0	-0.6	0
-0.7	0	-0.7	0	-0.7	0	-0.7	0
-0.8	0	-0.8	0	-0.8	0	-0.8	0
-0.9	0	-0.9	1	-0.9	1	-0.9	2
-1	5	-1	3	-1	10	-1	9

Summary and Conclusion

- A3PL Flash FPGAs have been subjected to a variety of environmental tests.
  - Small set of DUTs have been “baked” for over 17,000 hours at 150 °C.
  - Large set of DUTs have been “baked” at 3 temperatures for 270 days.
  - Outlier cells (~1%) have been tracked and are stable.
    - No new outliers have appeared after initial programming and margin testing.
- SmartFusion2 FPGAs: Started assessment.
- Supporting DMEA on use of EM analysis techniques.
  - EM: Electromagnetic signature analysis.
  - See D. Flowers’ paper, this conference.

References

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- "Viability of New COTS Technologies in Future Weapon Systems," J. Marchiondo, et. al, Sandia National Labs, September 2010.
- "High Reliability FPGAs in Fuze and Fuze Safety Applications," O'Neill, K., 59th Annual NDIA Fuze Conference, May 3-6, 2016, Charleston, South Carolina.
- "An Evaluation of Flash Cells Used in Critical Applications," R. Katz, D. Flowers, and K. Bergevin, 59th Annual Fuze Conference, May 3-6, 2016, Charleston, South Carolina.
- "Analysis & Recommendations for the Implementation of Flash Devices in Safety-Critical Applications," D. Flowers, and K. Bergevin, 59th Annual Fuze Conference, May 3-6, 2016, Charleston, South Carolina.
- "Digital Device Architecture and the Safe Use of Flash Devices in Munitions," R. Katz, D. Flowers, and K. Bergevin, 60th Annual Fuze Conference, May 9-11, 2017, Cincinnati, Ohio.
- "Advanced Analysis Techniques for the Implementation of Flash Devices in Safety-Critical Applications," D. Flowers, K. Bergevin, K. Islam, and M. Demmick, 60th Annual Fuze Conference, May 9-11, 2017, Cincinnati, Ohio.
- DoD Fuze Engineering Standardization Working Group, "Technical Manual for the Use of Logic Devices in Safety Features," March 8, 2011.